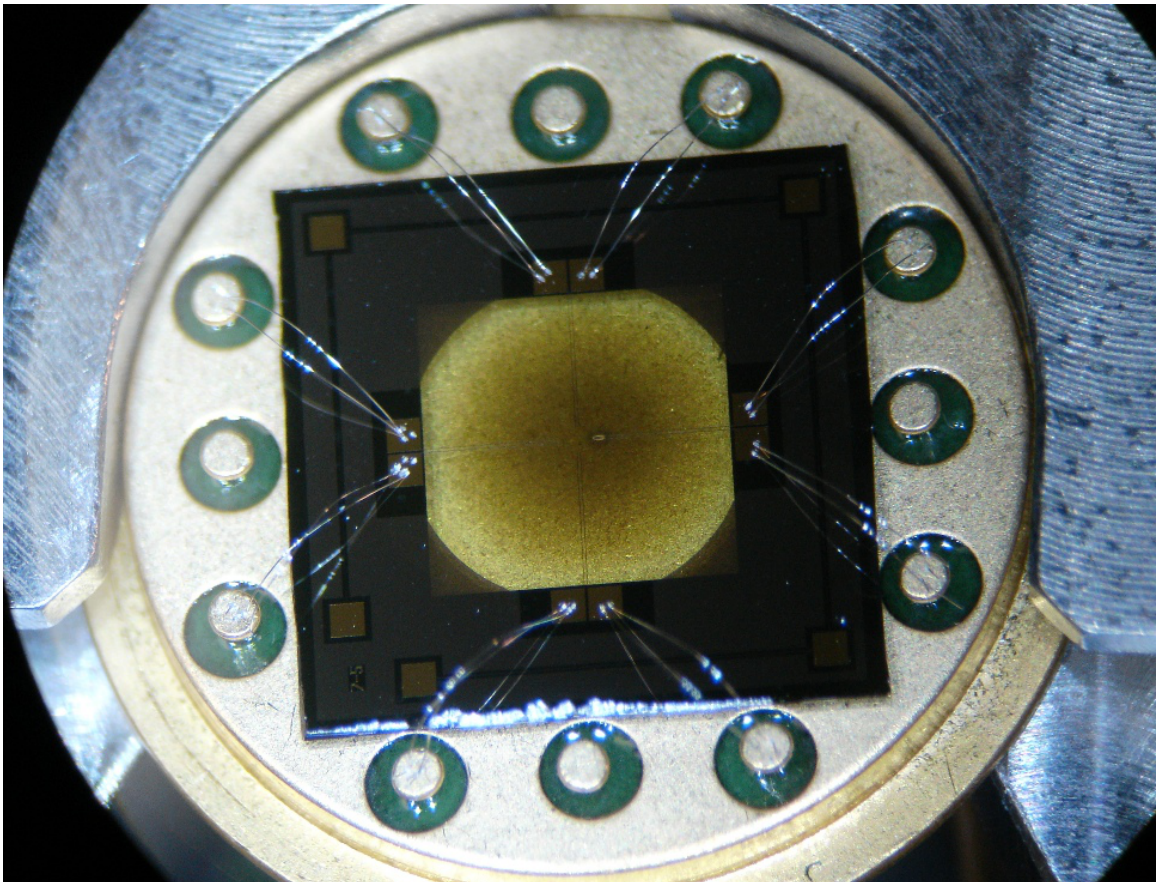

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Cover photograph A transition edge sensor using niobium as the superconducting thermometer bonded with Al wires for tests.

Development of A High-T_c Superconducting Transition Edge Sensor Detector

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A Thesis
Submitted to the School of Graduate Studies
of the University of Lethbridge
in Partial Fulfilment of the
Requirements of the Degree

Master

in

Science

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Abstract

This thesis describes design, fabrication, and characterizations of high-T_c transition edge sensor (TES) detectors aiming at cryogen-free infrared application. TES is a superconducting thermometer based bolometric detector, whose operating resistance is strongly dependent on temperature, and therefore shows much higher sensitivity than standard non-superconducting bolometers.

This thesis starts from the overview of major infrared detectors, then discusses in detail the theoretical background of a TES detector and some important figures of merit in evaluating its performance. Some TES arrays that are currently in use or under development for astronomical, ground or space-based missions are reviewed. The core of this thesis is the design and fabrication process of a TES detector, which is presented as a live report in Chapter 3 and provides useful guide for future detector fabrication. In order to evaluate performance of our devices, a cryogen-free cryostat is used for testing and its operational mechanics is introduced. In the final part, the experimental configurations for different tests are delivered, and the figures of merit mentioned above are measured and used to characterize fabrication results.

Acknowledgements

First, I need to thank my supervisor, Professor David Naylor for offering me such a great opportunity to fulfill my dream of becoming a professional engineer. When I first joined the group, I had been away from my undergraduate specialty for many years and cannot help to worry if I could finish the degree. After my so many times' mistakes, such as breaking a detector arrived far away from UK, and most recently venting the helium gas from the cryostat, David still tolerated and encouraged me with his great patience and broad heart. To find a project that fits for my undergraduate specialty and also to help me to more conveniently visit my husband, who was working at University of Alberta, David provided me an inspiring opportunity to study nanofabrication technology and make TES detectors in University of Alberta's Nanofab. Not only did this become the starting point and core of this thesis, but also opened a door to entirely new techniques and for my future profession. After all of these, David even offers me a contract to make new detectors after my graduation, which will help me a lot in settling down and preparing for future career. I hope someday, even I cannot be comparable to David in success, I can still become a person like him, who makes everyone around him work delightedly and feel to be respected.

I am especially grateful for my husband, who has always been supportive and never complain about my busy study and being a commuter couple. Whenever and wherever, I know you are there, I feel this is home.

To my parents in China, after have being away from home for 3 years yet never been able to go back, I miss you so much and feel so guilty. I should have stayed with you and taken care of you, but it is me who has been cared for since I was a child. I hope this

thesis could be the best gift to you when I return home.

I also need to thank all the group members, to Darren, who has been so patient to instruct me step by step and taught me not only techniques but most importantly the careful and responsible attitude in work; to Brad, who is very helpful in both my thesis and experiments, and every time I went for his help I know there is an answer; to Greg, who helps me a lot in circuit design and instrument operation; to Gibion, who gave me generous help even when he was also busy with thesis, and his hard work also inspired me a lot; to Locke, Richard, and Scott, who were always willing to listen to my questions and answer them.

I would like to thank the director Dr. Ken Westra and all the staff in the Nanofab of University of Alberta for the aiding in our fabrication process, and to CMC Microsystems for financial support of both fabrication and traveling.

Contents

List of Tables

List of Figures

List of Equations

Chapter 1

Introduction

Since the year of 1800 for the first time the infrared (IR) radiation was observed by Sir William Herschel's prism experiment, efforts in exploring the infrared region have been progressively continued. The nineteenth century witnessed some pioneering milestones, such as the discovery of the thermoelectric effect [1],the invention of bolometer [2], and the first attempt of detecting infrared radiation from a star [3]. However, it was not until the 1960s, that the development of modern infrared technology exploded, which led to the foundation of modern infrared astronomy [3]. Since that time, the growing demands of astronomical applications have been the driving force for infrared detector technology [4]. In this chapter, I will briefly introduce the background of infrared astronomy, the application of infrared detectors in modern astronomy, major types of infrared detectors, and some important figures of merit in evaluating their performance.

1.1 Overview of Infrared Astronomy

In the field of astronomy, the infrared spectral region between wavelengths of 1 - 1000 μm [5] is of special importance as it contains abundant information from the Universe. As shown in Figure 1.1, many astronomical sources radiate over a broadband wavelengths at the infrared region. In the near-IR region (1-5 μm) [6] lies radiation from red stars and warm dust. In the mid-IR region (5-30 μm) [6] warm dust emission dominates. In the far-IR region (30-300 μm) [6] lies emission from planets and interstellar cold dust. In the sub-millimeter (300-1000 μm) [6] region the cosmic microwave background (CMB) resulting from the Big Bang can be observed. Observations at infrared wavelengths allow us to study the formation and evolution of galaxies, stars, and planets. Unlike visible radiation which is mostly blocked by dust, infrared radiation can easily penetrate these dust and therefore deliver abundant astronomical information. Today, the infrared spectral region has become a major focus of international astronomical research. Many infrared astronomical observatories are either in operation or under-development. The recently launched Herschel Space Observatory (in 2009) carries three instruments onboard: PACS (Photodetector Array Camera and Spectrometer), SPIRE (Spectral and Photometric Imaging Receiver), and HIFI (Heterodyne Instrument for the Far Infrared); all these instruments operate at infrared regions covering from the far-IR to sub-millimeter [7]. Another proposed mission, SPICA (Space Infrared Telescope for Cosmology and Astrophysics), will cover the full mid-IR and far-IR region with three instruments: a mid-IR coronagraph, a mid-IR camera and spectrometer, and SAFARI (SPICA Far-infrared Instrument) - a far-IR imaging spectrometer.

Besides all the attractions and opportunities, infrared observations are also accom-

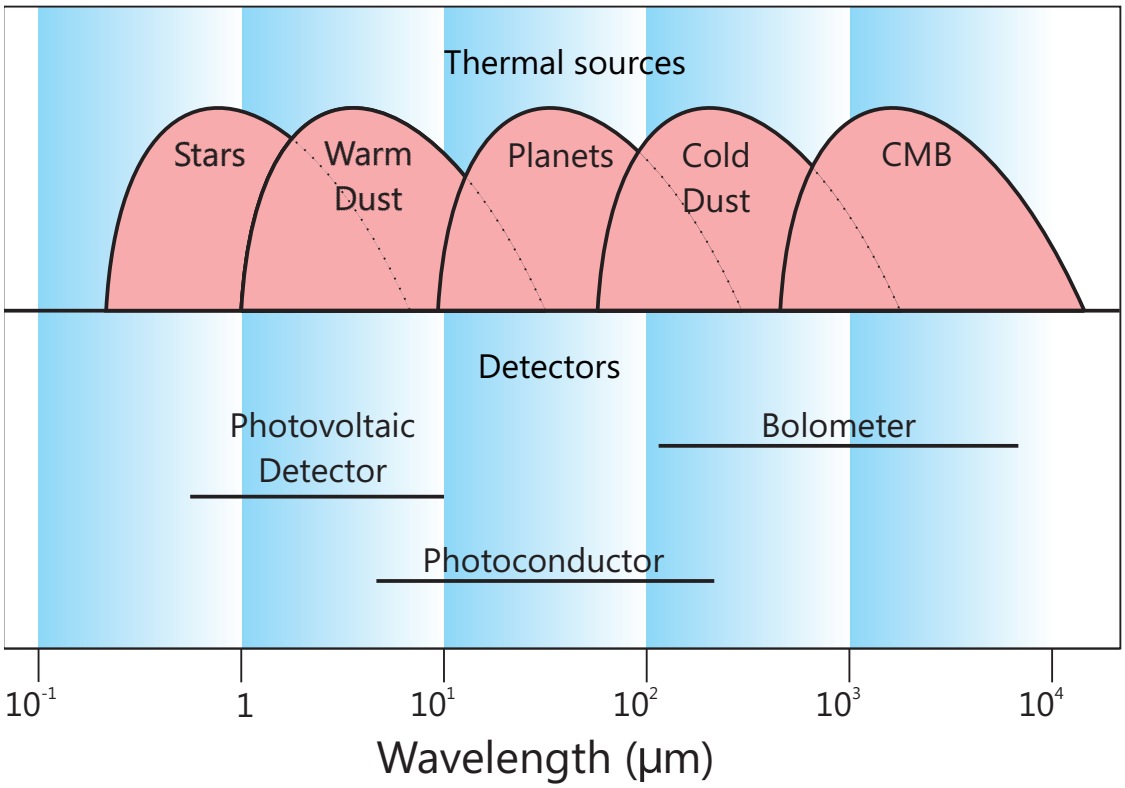

Figure 1.1: Dominant sources radiating at different wavelengths at the IR region and the preferred detectors for each wavelength band [5].

panied by challenges. One is the limited wavelength bands for ground-based observations, as water vapor, carbon dioxide, and ozone absorb infrared radiation when it enters the atmosphere of the earth. For this reason, many infrared telescopes are launched into space.

One of the most critical component of all astronomical instrumentation is the sensitive detector. Not only is the performance of a single device required, but also the number of pixels that can be packed into an array. Efforts in optimizing infrared detectors and developing new devices have been on-going, indeed every new astronomical mission places an increasingly more stringent requirement on detector performance. The next sections will focus on the major types of infrared detectors and introduce important figures of merit to

evaluate their performance.

1.2 Overview of Infrared Detector

Infrared detectors absorb incoming photons from the astronomical source and convert them into meaningful signals. Infrared detectors can be grouped into two main types: photon detectors and thermal detectors [8].

A photon detector responds directly to an incoming photon which excites free charge carriers in the detector. The wavelength response of the photon detector is determined by the bandgap energy of the detector material, as given by the following expression:

$$\frac{hc}{\lambda} \geq E_g \ , \tag{1.1}$$

where $h \ = 6.626 \times 10^{34} \quad [J \cdot s]$ is Planck's constant, $c \ = 2.998 \times 10^8$ $[m \cdot s^{-1}]$ is the speed of light, and λ [m] is the wavelength of incoming photons. Equation 1.1 indicates that a photon detector can only respond up to a cutoff wavelength, $\lambda_{co} = hc/E_g$. Photoconductors, photovoltaic detectors, and photoemissive detectors are typical examples of photon detectors.

A thermal detector does not respond directly to incoming photons, but rather, the radiation is absorbed by the detector substrate and and the resulting small change in temperature of the substrate is measured by a sensitive co-located thermometer. The response of thermal detector is therefore not limited by the wavelength of incoming photons and can achieve a broad spectral coverage. The most common types of thermal detectors are bolometer, pyroelectric detector, and thermoelectric-effect detector (thermocouple and thermopile). This thesis focuses on the transition edge sensor (TES), a bolometer based on

the superconducting thermometer.

1.3 Figures of Merit

Figures of merit are quantities that characterize the performance of an infrared detector. Some commonly used figures of merit include noise equivalent power (NEP), responsivity (R_i or R_v), detectivity (D^*), and time constant (τ), which will be discussed in this section. These figures of merit are useful not only in predicting the detector's performance in a given application, but also for comparing the performance of one detector with another.

1.3.1 Noise Equivalent Power

The noise equivalent power (NEP) expresses the sensitivity of an infrared detector. The NEP is the incident power (P_s) on a detector that yields an rms signal-to-noise ratio (SNR) of unity, with the unit of W. The NEP is normalized to the frequency bandwidth of 1 Hz, and has the unit $W/\sqrt{Hz}$. The smaller the NEP, the more sensitive the detector. The NEP can be expressed as [8]:

$$NEP = \frac{P_s}{SNR\sqrt{\Delta f}} \quad [W/\sqrt{Hz}], \tag{1.2}$$

where Δf is the electronic noise bandwidth.

1.3.2 Responsivity

Responsivity is the ratio of the output electrical signal (voltage or current) to the incident optical power. It can be expressed as either current responsivity (R_i) or voltage

responsivity (R_v) depending on the actual type of detector:

$$R_i = \frac{I}{P_s} \quad [A/W], \tag{1.3}$$

$$R_v = \frac{V}{P_s} \quad [V/W], \tag{1.4}$$

where I and V are the output current and output voltage, respectively.

If the detector is limited by current or voltage noise, the NEP can be expressed in terms of responsivity by substituting Equation 1.3 and Equation 1.4 into Equation 1.2, respectively:

$$NEP = \frac{I_n}{R_i} \quad [W/\sqrt{Hz}], \tag{1.5}$$

$$NEP = \frac{V_n}{R_v} \quad [W/\sqrt{Hz}], \tag{1.6}$$

where I_n (in $A/\sqrt{Hz}$) is the output noise current and V_n (in $V/\sqrt{Hz}$) is the output noise voltage.

1.3.3 Detectivity

Detectivity, or more specifically normalized detectivity, D^*, is the reciprocal of normalized NEP multiplied by the square root of the detector area [8]:

$$D^* = \frac{\sqrt{A_d}}{NEP} \quad [cm \cdot \sqrt{Hz}/W], \tag{1.7}$$

where A_d is the detector area. The normalized detectivity can be used to compare performances of detectors of different sizes measured under different noise bandwidth.

1.3.4 Frequency Response

In most cases, the incident optical power is modulated by either chopper or other modulation scheme into a sine- or square-wave signal. The frequency response of an infrared detector describes the dependence of the signal output on the frequency of the modulated input signal. The frequency response is determined by the response time, or time constant. By analogy to an electrical RC circuit, $\tau = RC$. In our tests (see Chapter 6), the time constant is determined at the -3 dB point, where

$$\frac{|V_{out}|}{|V_{out\_DC}|} = \sqrt{2}, \tag{1.8}$$

so

$$20log\frac{|V_{out}|}{|V_{out\_DC}|} = -3 \quad [dB]. \tag{1.9}$$

Here $|V_{out}|$ is the amplitude of Fourier transformed output voltage of the detector in the frequency domain, and $|V_{out\_DC}|$ is the value of $|V_{out}|$ at low frequency (DC). The corresponding frequency at -3 dB point is the cutoff frequency.

Therefore, time constant τ can be derived from the cutoff frequency equation:

$$f_{co} = \frac{1}{2\pi\tau} \quad [Hz], \tag{1.10}$$

so time constant τ is:

$$\tau = \frac{1}{2\pi f_{co}} \quad [s]. \tag{1.11}$$

1.4 Thesis Outline

Chapter 2 introduces the structure, operational mechanics of a TES detector and some important parameters that affect its design and performance. TES arrays that are currently in use or under development for astronomical, ground or space-based missions are also reviewed. Chapter 3 is the core of this thesis and describes the fabrication process of our TES devices. From the design of the lithography masks to the microfabrication techniques, each step is presented in detail and includes: descriptions, illustrations, recipes, and application notes for future reference. Chapter 4 describes the operational mechanics of the cryostat system used to test the detectors. Chapter 5 describes the experimental configuration used to test performance of the detectors. Chapter 6 presents the results from the experimental tests that have been performed on the TES detectors including: Resistance-temperature, noise, and frequency response measurements. Analysis and interpretation of these results are presented.

Chapter 2

The Transition Edge Sensor

2.1 Introduction

The transition edge sensor (TES) is a type of bolometer, which is based on a superconducting thermometer. The superconducting thermometer operates over a very narrow region around its transition temperature, T_c, where its resistance changes sharply from superconducting to its normal value. This extremely strong dependence of resistance on temperature results in a dramatic change in signal for a very small amount of absorbed incident power.

In the following sections, I discuss the structure, operational mechanics, and important parameters that affect the design and performance of a TES detector; I will also review several TES arrays that are currently in use or under development for astronomical, ground or space-based missions.

2.2 Theoretical Background

In this section I will outline the fundamental operational principles of a bolometric detector.

2.2.1 Structure and Components

Figure 2.1 shows the structure of a simple TES detector which consists of three main components: a superconducting thermometer attached to an absorber, a heat sink, and a weak thermal link connecting the thermometer with the heat sink. The performance of the detector is determined by the values of the following parameters: the transition temperature T_c [K] of the superconducting thermometer, the heat capacity C [J/K] of the absorber, the thermal conductance G [W/K] of the thermal link, and the base temperature T_0 [K] of the heat sink.

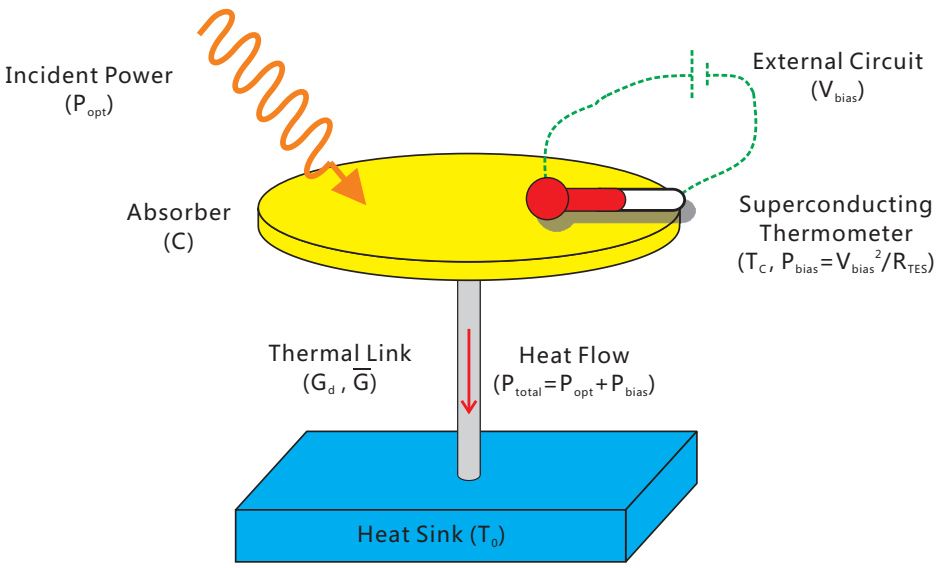

Figure 2.1: The basic structure of a TES detector.

2.2.2 Operation Mechanics

Although the TES is a superconducting bolometer, its principle of operation is essentially the same as any conventional bolometer based on a non-superconducting thermometer. Incident power is absorbed and thermalized by the absorber, which increases the temperature of the thermometer. Since the electrical resistance of the thermometer is a steep function of temperature, the resistance increases; and an external readout circuit converts the resistance changes into electrical signals from which the incident power can be derived.

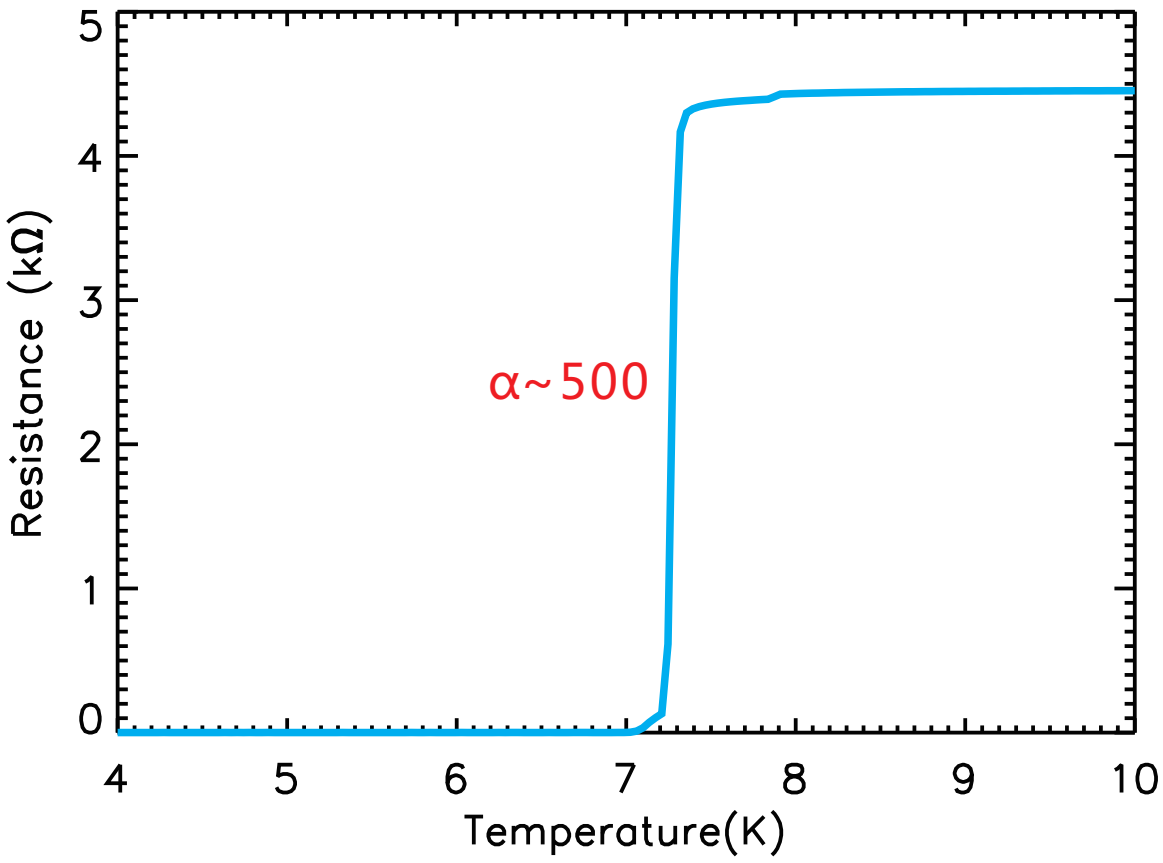

Figure 2.2: The sharp resistive transition of a 20 nm thick Nb thermometer at ∼7.25 K results in a high sensitivity detector; α is the logarithmic sensitivity.

The TES detector, however, can operate with a much higher optical sensitivity than a non-superconducting bolometer as its superconducting thermometer shows a much stronger temperature dependence of resistance than the latter. As shown in Figure 2.2, at the very narrow region around the transition temperature T_c, the resistance of a superconducting thermometer changes extremely sharply from superconducting to normal status; therefore, if a TES can be operated within this narrow region, even a very small amount of incident power can dramatically change its resistance and therefore be detected.

The strong temperature dependence of resistance shown in Figure 2.2 can be quantitatively described by the logarithmic sensitivity, α [9]:

$$\begin{aligned} \alpha &= \frac{\mathrm{d}(\log R)}{\mathrm{d}(\log T)} \\ &= \frac{\mathrm{d}(\log R)/\mathrm{d}T}{\mathrm{d}(\log T)/\mathrm{d}T} \\ &= \frac{(1/R)\log e(\mathrm{d}R/\mathrm{d}T)}{(1/T)\log e} \\ &= \frac{T}{R}\frac{\mathrm{d}R}{\mathrm{d}T}. \end{aligned} \tag{2.1}$$

The value of a TES detector's sensitivity shown in Figure 2.2 is around 500; this is to be compared with typical values of around 10 for non-superconducting bolometers. The increased sensitivity of the TES arises from the steepness of the superconducting transition. While it may seem challenging to maintain the TES operating point at the mid point of the transition, in practice this is readily achieved by the use of voltage-biased read out circuit [10].

2.2.3 Voltage-bias and Negative Electrothermal Feedback

In a typical non-superconducting bolometer, resistance decreases with increasing temperature. Such bolometers are usually biased with a constant current; when the incident power raises the temperature of the bolometer, its resistance drops and so does the dissipated bias power $P_{bias} = I^2{}_{bias}R$, which compensates for the incident power. If a TES were to be operated in a current-biased mode, its resistance would increase with increasing temperature, and so too the dissipated bias power, which would lead to thermal runaway. By operating the TES in a voltage-biased mode, the dissipated bias power becomes $P_{bias} = V^2{}_{bias}/R$, which decreases with increasing resistance. The opposing effect of dissipated bias power on temperature, known as negative electrothermal feedback (ETF), allows the TES to self-bias at a stable temperature point in the transition region. The strength of the ETF is given by [11]:

$$L = \frac{P_{bias}\alpha}{G_d T_c}, \tag{2.2}$$

where L is the loop gain in analogy to electronic feedback circuits, P_{bias} is the dissipated bias power in the TES, α is the logarithmic sensitivity, $G_d = dP/dT$ is the dynamic thermal conductance, and T_c is the thermometer temperature.

The negative ETF also helps to improve the response speed. The response time, or time constant, τ, of a voltage-biased TES with the negative ETF is given by [11]:

$$\tau = \frac{\tau_0}{1+L}, \tag{2.3}$$

where $\tau_0 = C/G_d$ is the intrinsic time constant without ETF. It is clear from Equation 2.3 that with a strong electrothermal feedback $L \gg 1$, the response time can be greatly reduced.

Another benefit from the large ETF is the high linearity of the responsivity. The current responsivity, R_i, of a voltage-biased TES is given by [11]:

$$R_i = -\frac{L}{V_{bias}(1 + L + i\omega\tau_0)}, \tag{2.4}$$

where V_{bias} is the bias voltage, and ω is angular frequency of the modulated incident power. At modulation frequencies much lower than the detector's maximum frequency response and with the strong ETF, the current responsivity can be simplified as [11]:

$$R_i \approx -\frac{1}{V_{bias}}. \tag{2.5}$$

Since in this case the current responsivity R_i is dependent only on bias voltage, it allows fabrication of multi-pixel TES array of uniform response.

2.2.4 Current-amplifier Readout Circuit

JFET or MOSFET amplifier readout circuits are commonly used for semiconductor bolometers and could, in principle, be used with TES of high resistance. In general, TES have low resistance, typically a few mΩ, in which case, the impedance of JFET or MOSFET amplifier introduces an unwanted source of noise. To circumvent the problem, a low-impedance current amplifier based on a Superconducting Quantum Interference Device (SQUID) is normally employed [10]. An alternative to SQUID for low-resistance TES is a transformer-coupled amplifier circuit [12].

The TES devices made by our group have normal resistances in the range from a few hundred ohms to a few kΩ, which allows us to use a simple operational-amplifier circuit without introduce a noise (see Appendix A). We have also explored the use of a transformer-coupled amplifier circuit, which allows us to use TES bolometers of lower resistances.

2.2.5 Heat Flow Analysis

The thermal equilibrium of a TES is established when the power flowing into the bolometer equals the total power flowing out to the heat sink through the thermal link, as shown in Figure 2.1:

$$P_{total} = P_{opt} + P_{bias}, \tag{2.6}$$

where P_{opt} is the absorbed incident optical power (from both the signal and the background noise) and P_{bias} is the bias power dissipated in the TES.

The power law equation for the total heat flow to the heat sink can be expressed as [13]:

$$P_{total} = K(T^n - T_0^n), \tag{2.7}$$

where T is the temperature of TES thermometer and T_0 is temperature of the heat sink. K and n are parameters that are related to the dynamic thermal conductance by:

$$G_d = \frac{dP_{total}}{dT} = nKT^{n-1}. \tag{2.8}$$

From Equation 2.8, K can be expressed as:

$$K = \frac{G_d}{n(T^{n-1})}. \tag{2.9}$$

Substituting Equation 2.9 into Equation 2.7, yields:

$$P_{total} = \frac{G_d}{n(T^{n-1})}(T^n - T_0^n). \tag{2.10}$$

The heat flow P_{total} can also be expressed in terms of the average thermal conductance $\bar{G}$:

$$P_{total} = \bar{G}(T - T_0). \tag{2.11}$$

Substituting Equation 2.11 into Equation 2.10 relates $\bar{G}$ and G_d:

$$\bar{G}(T - T_0) = \frac{G_d}{n(T^{n-1})}(T^n - T_0^n). \tag{2.12}$$

If the incident optical power P_{opt} is constant, then Equation 2.8 can be rewritten as:

$$G_d = \frac{d}{dT}(P_{opt} + P_{bias}) = \frac{dP_{bias}}{dT}. \tag{2.13}$$

Equation 2.13 provides a practical method of determining the dynamic thermal conductance G_d. One simply measures the slope of the dissipated bias power as a function of the TES thermometer temperature, the slope then equals G_d.

2.2.6 Noise Analysis

The total noise when using a TES bolometer is the quadrature sum of several uncorrelated noise sources, including photon noise, thermal fluctuation noise (phonon noise), Johnson noise, and preamplifier noise, and is given by:

$$NEP^2 = NEP^2_{photon} + NEP^2_{thermal} + NEP^2_{Johnson} + NEP^2_{preamp}. \tag{2.14}$$

Photon noise describes the Poisson statistical fluctuation of the incoming photons on a detector and can be expressed as [14]:

$$NEP^2_{photon} = 4A\Omega\alpha\epsilon f\frac{k^5T_s^5}{h^3c^2}\int\frac{x^4}{e^x-1}(1+\frac{\alpha\epsilon f}{e^x-1})dx, \tag{2.15}$$

where $k = 1.38\times10^{-23}$ $[J\cdot K^{-1}]$ is Boltzmann's constant, $h = 6.626\times10^{34}$ $[J\cdot s]$ is Planck's constant, $c = 2.998\times10^8$ $[m\cdot s^{-1}]$ is the speed of light, α is the absorptivity of the detector, ϵ and T_s are the emissivity and temperature of the radiation source respectively, f and $A\Omega$ are the transmissivity and throughput of the optical system respectively, and $x = h\nu/kT_s$ where ν is the frequency of modulated incident power.

Thermal fluctuation noise or phonon noise arises from energy fluctuations along the thermal link from the TES thermometer to the heat sink. For a well-designed TES the thermal fluctuation noise should be the dominant source of noise as given by [14]:

$$NEP^2_{thermal} = \gamma 4kT^2G_d. \tag{2.16}$$

Here $\gamma \approx 1-(1+n/2)t+(2+n)(2+3n)t^2/12$, where $t = 1-T_0/T$, T_0 and T are temperature of the heat sink and the TES thermometer, respectively.

Johnson noise arises from the resistive property of the TES. With the existence of ETF, Johnson noise is given by [15]:

$$NEP^2_{Johnson} = \frac{4kT/R}{|R_i|^2}\Big(\frac{\tau}{\tau_0}^2\Big)\Big(\frac{1+\omega^2{\tau_0}^2}{1+\omega^2\tau^2}\Big), \tag{2.17}$$

where k is Boltzmann's constant, T and R are temperature and resistance of the TES, respectively, R_i is the current responsivity (Equation 2.4), τ_0 and τ are the intrinsic time constant without ETF and the effective time constant with ETF (Equation 2.3), respectively.

Preamplifier noise is electrical noise related to specific bias and readout circuits. Besides the major noise sources discussed above, there is still excess noise such as 1/f noise, pick-up noise and harmonic noise from electrical devices.

2.3 Design Considerations

Performance of a TES, such as NEP and response speed, is directly connected with its design and structure, or more specifically with the four important intrinsic parameters: transition temperature T_c, heat sink temperature T_0, heat capacity C and thermal conductance G. In this section we will discuss in detail the theories and schemes in employing these parameters to design a TES.

2.3.1 Transition Temperature Control

The transition temperature, T_c, of the superconducting thermometer is the most critical parameter in determining design and performance of a TES, as the thermal fluctuation noise (Equation 2.16) is directly related to it, and other important parameters such as heat capacity and thermal conductance are also dependent on it. The cryogenic system also needs to be compatible with the transition temperature. Therefore, the first step of designing a TES detector is to select a suitable superconducting material and tune its transition temperature to the desired value.

There are three ways to control T_c: Making a proximity-effect multilayer of normal metal and superconductor, doping the superconductor with magnetic ions, and controlling the thickness of an intrinsic superconductor [10]. The proximity-effect multilayer is com-

prised of one or more normal/superconductor bilayers. It employs the proximity-effect between the normal layer and the superconductor layer to suppress the transition temperature than the intrinsic transition temperature of the superconductor. By varying the thickness of the metal layers, T_c can be tuned to different values. The proximity-effect multilayer is the most widely used method to control T_c [10]. T_c can also be suppressed by adding a small amount of magnetic dopants such as Fe ions into a superconductor [10].

Our group uses the third method; depositing thin Nb films of different thickness to get T_c in the range of about 4-9 K, while the bulk value of T_c of Nb is 9.2 K. This method is based on the fact that for Nb films thinner than 100 nm the transition temperature drops as film thickness decreases, and this change is especially noticeable for film thickness below 50 nm [16]. We have verified this thickness dependence of T_c and the results are presented in Chapter 6.

2.3.2 Thermal Link Design

The thermal conductance of the thermal link between the thermometer and the heat sink is another important parameter that can significantly affect the performance of a TES as both the thermal fluctuation noise (Equation 2.16) and response time τ (Equation 2.3) are directly dependent on it. These two equations imply a low thermal conductance as the rule of design. However, Equation 2.11 also indicates that the lower the average thermal conductance is, the easier a detector can be saturated by incident power. Therefore, the lower boundary of thermal conductance is set by the estimated power load. A widely used method to achieve a low thermal conductance is to fabricate a Si_3N_4 structure between the TES thermometer and the heat sink as a weak thermal link [10]. A solid Si_3N_4 membrane

(Figure 2.3) is the basic thermal structure, and mesh Si_3N_4 structures can further reduce thermal conductance by reducing the cross-section area of the thermal link. Different mesh structure schemes have been experimentally studied by many groups ([11], [17], [18], [19]), an example of a spiderweb structure is shown in Figure 2.4. The packing density can be improved by a squared geometry as shown in Figure 2.5. Figure 2.6 shows other varieties of the mesh grid structure; the noticeable differences are the very high length to cross-section aspect ratio of the Si_3N_4 support beams, which result in even lower thermal conductance [18], [19].

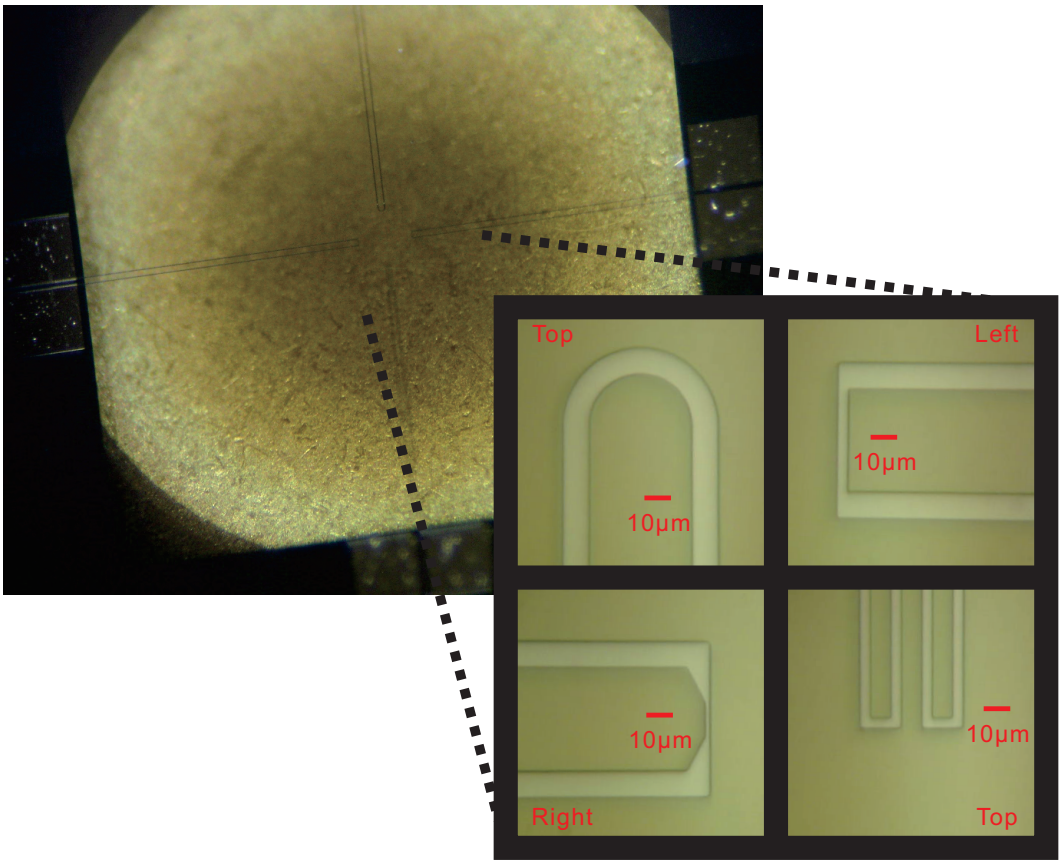

Figure 2.3: Photograph of a solid Si_3N_4 membrane TES and microscopic graph of Nb Sensors (fabricated by University of Lethbridge). Nb Sensors and leads are extended to the center, and Au absorber (dark circle) is directly deposited onto the membrane.

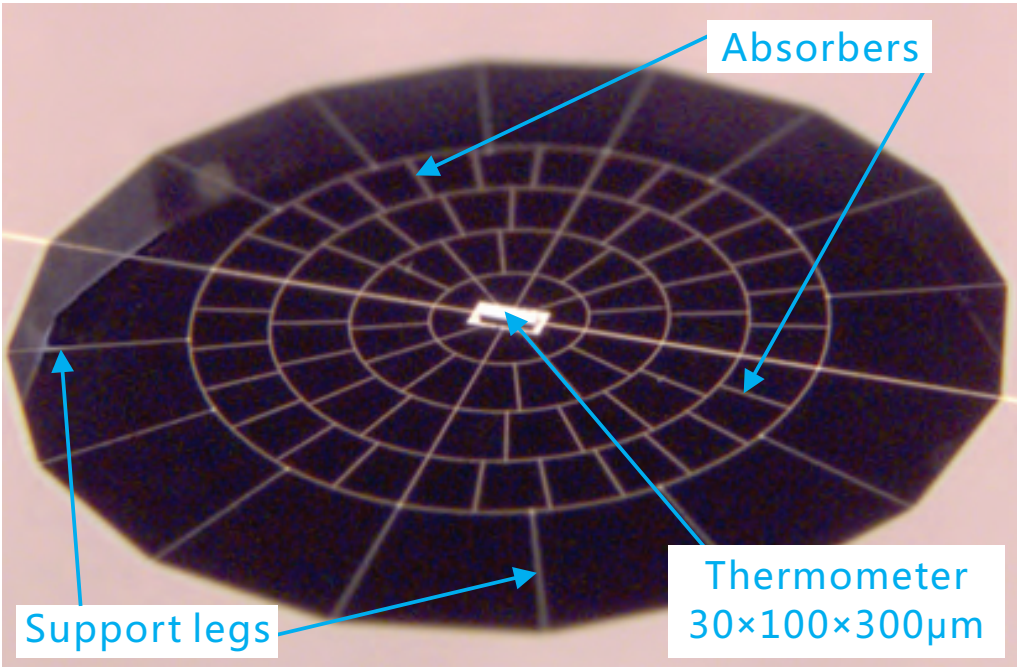

Figure 2.4: Photograph of the spiderweb bolometer of the high frequency instrument (HFI) aboard the Planck satellite [18]. The thermometer is made by semiconductor instead of superconductor though and the circular mesh Si_3N_4 structure is metalized as absorbers.

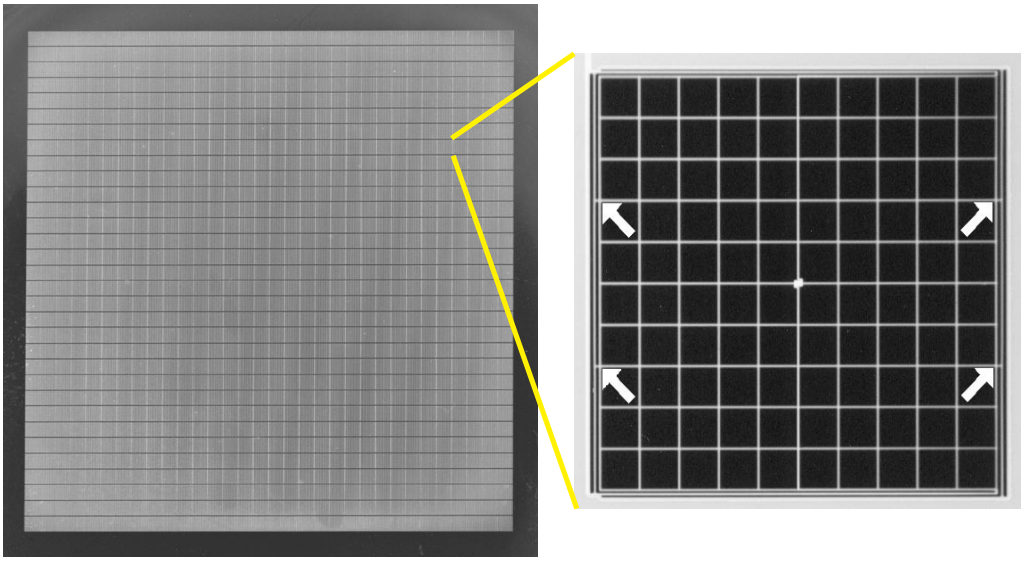

Figure 2.5: Photographs of a mesh grid structure TES array (Left) and a magnified single pixel (Right) [17]. The absorbers are also made by metalizing the Si_3N_4 grid mesh.

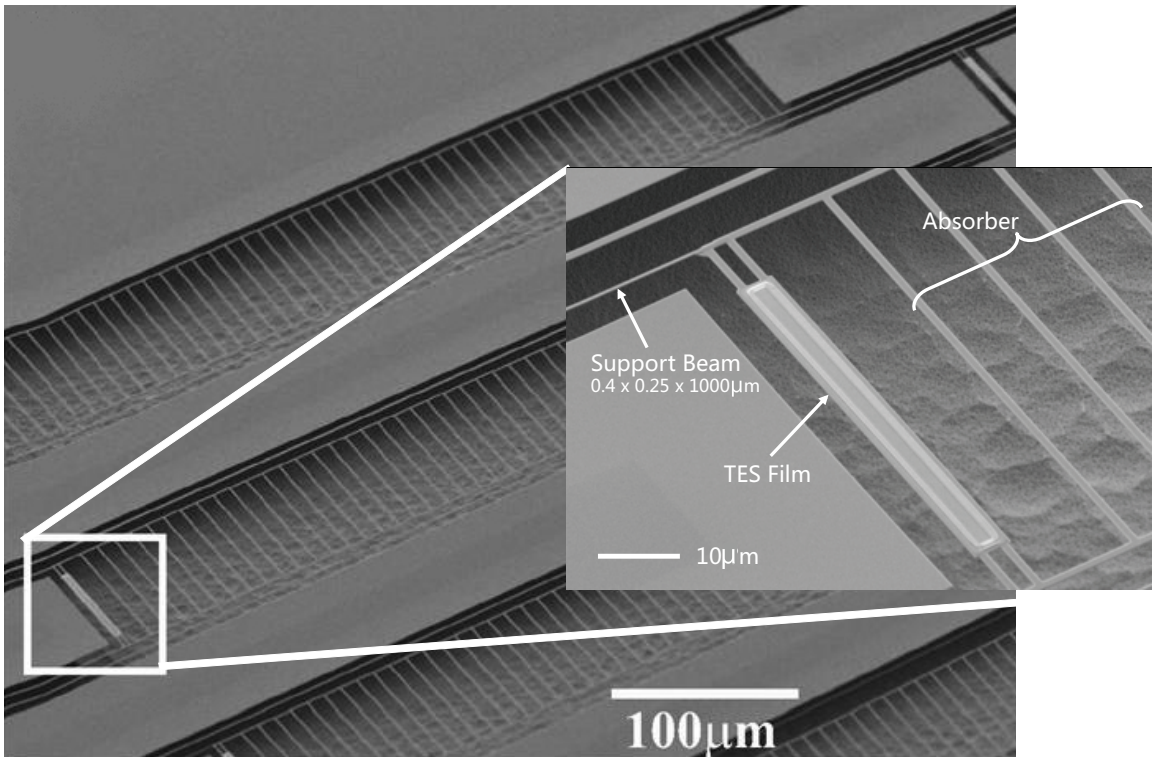

Figure 2.6: Photographs of a TES prototype designed for BLISS [18], [19]. The absorbers are a group of paralleled metal wires on top of the Si_3N_4 grid mesh.

2.3.3 Absorber Design

An efficient absorber should have a high absorptivity to incident optical power and also a small time constant for thermalizing optical power into heat. The absorptivity can be maximized by good thermal coupling methods, which will be discussed later in this section. The thermal time constant of the absorber places a limit on the response time of a TES device, therefore, it is more important to reduce the heat capacity of the absorbing membrane than the heat capacity of the TES itself. A low heat capacity can be achieved by fabricating absorbers with low heat capacity materials such as Au (Figure 2.3), or with mesh structures. The latter is usually realized by directly metalizing the Si_3N_4 mesh structures

which then become the absorbing membrane (Figure 2.4, 2.5, 2.6).

There are four common methods to couple incident power to the TES at the far-infrared to millimeter wavelength region. For wide band applications, direct absorber coupling can be used as long as the absorber material matches the impedance of free space. For a narrow band application, the absorber coupled with a quarter-wavelength backshort is more efficient. Spiderweb TES detectors are usually coupled with feedhorns which include an integrating cavity to further improve the absorption. Another method is to use antenna-coupling to the TES through microstrip transmission lines [10].

2.4 Review of TES

In this section we review some TES devices that have been implemented or under development for notable astronomical and ground-based astronomy missions.

In 2001, the FIBRE (Fabry-Perot Interferometer Bolometer Research Experiment) broadband submillimeter spectrometer on Caltech Submillimeter Observatory (CSO) started operation [20]. It is comprised of two 1×8 Mo-Cu bilayer TES arrays (Figure 2.7) which used a SQUID multiplexer readout. This represented the first application of a multiplexed TES array in astronomy. The design of the FIBRE TES consisted of a pop-up structure that was enabled by folding the support legs behind the absorbers, which resulted in a compact-packed 2D array (Figure 2.9) [10], [21]. In 2006, the Multiplexed SQUID/TES Array for Ninety GHz (MUSTANG) was commissioned on the 100 m Green Bank Telescope (GBT) [22], [23]. In 2007, the Goddard IRAM Superconducting 2 Millimeter Observer (GISMO) instrument on the IRAM 30 meter telescope in Spain achieved first light. GISMO consisted

of a 8×16 TES array with a Backshort Under Grid (BUG) structure as a quarter-wavelength reflective backshort placed behind detectors to increase the optical efficiency [24]. In the same year of 2007, the APEX-SZ TES array receiver (Figure 2.8) on the APEX Telescope began to survey the galaxy clusters. This instrument consists of 320 feedhorn-coupled Al-Ti bilayer TES pixels with T_c of ∼450 mK; the absorber is a Au spiderweb [25]. 2007 also saw the start of observations with the Millimeter Bolometer Array Camera (MBAC) to study the cosmic microwave background (CMB) on the Atacama Cosmology Telescope (ACT). This instrument used three 32×32 pop-up Mo-Au TES arrays (Figure 2.9) for different wavelength bands [26]. In 2010, the SCUBA-2 camera was installed operation on the James Clerk Maxwell Telescope (JCMT) for observations at the two wavelengths: 450 and 850 μm [27]. SCUBA-2 employs more than 10,000 Mo-Cu bilayer TES pixels which are directly bump-bonded with SQUID multiplexer readout electronics (Figure 2.10) [28].

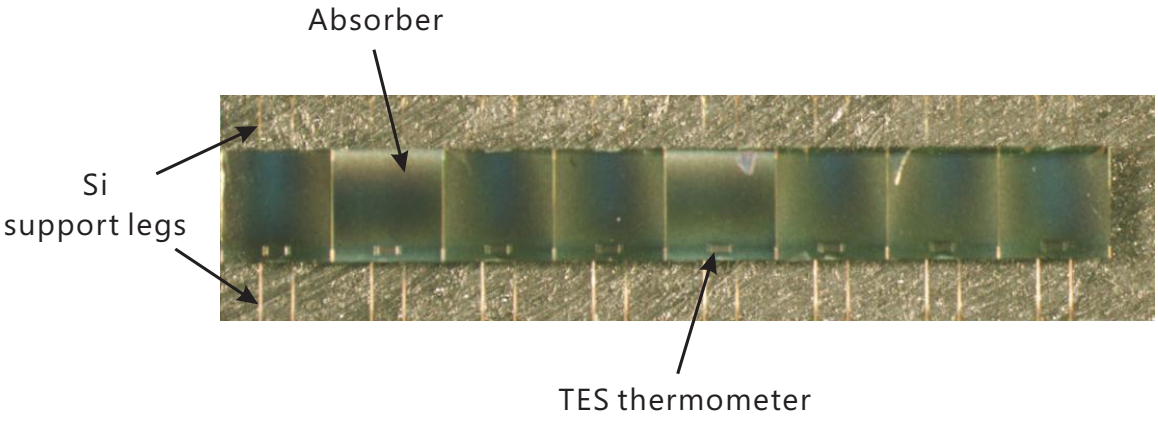

Figure 2.7: Photograph of a 1×8 TES array used in FIBRE [29].

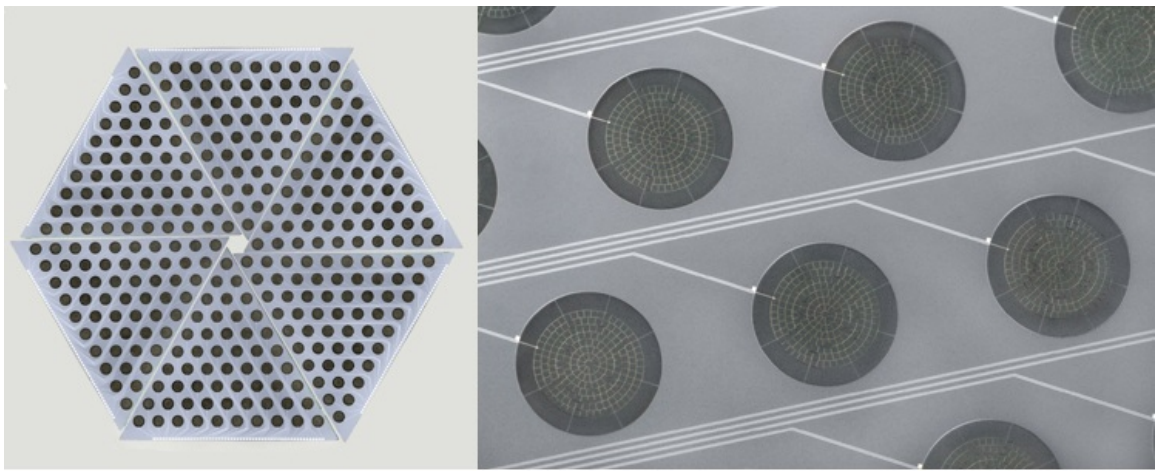

Figure 2.8: Left: photograph of the 320-pixel APEX-SZ TES array. Right: magnified single spiderweb TES pixels [30].

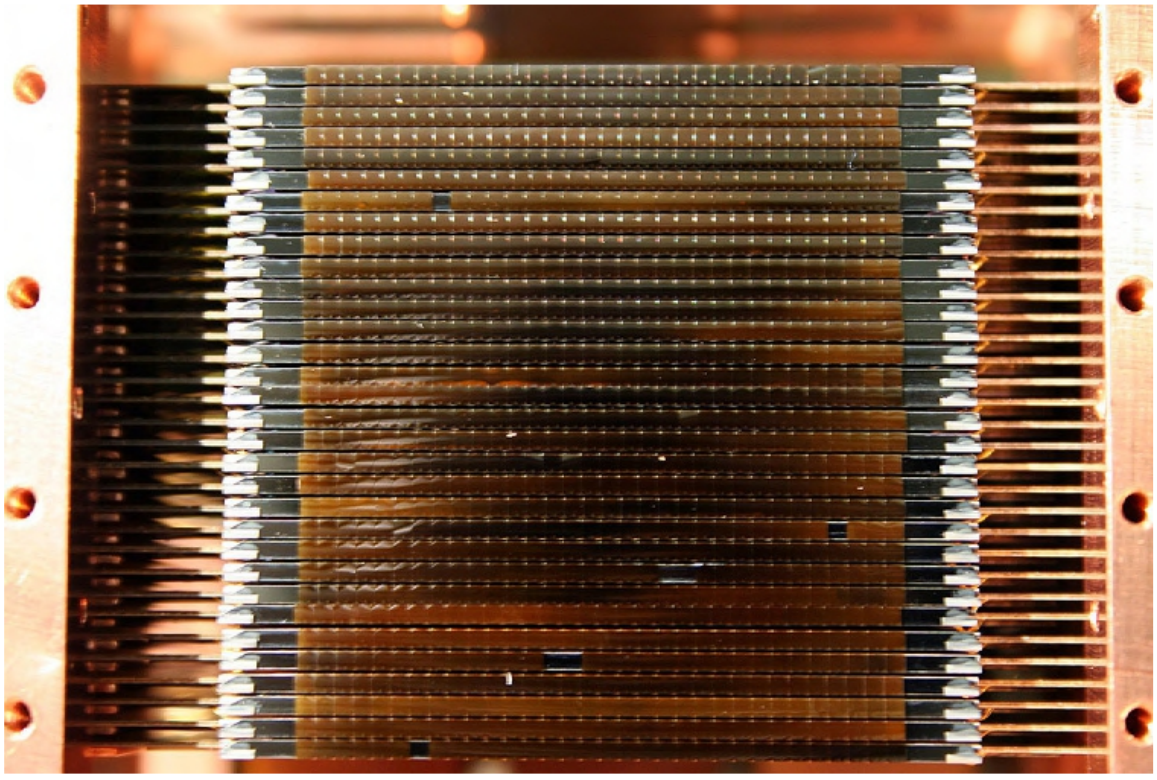

Figure 2.9: Photograph of the stacked 32×32 pop-up TES arrays in MBAC [31].

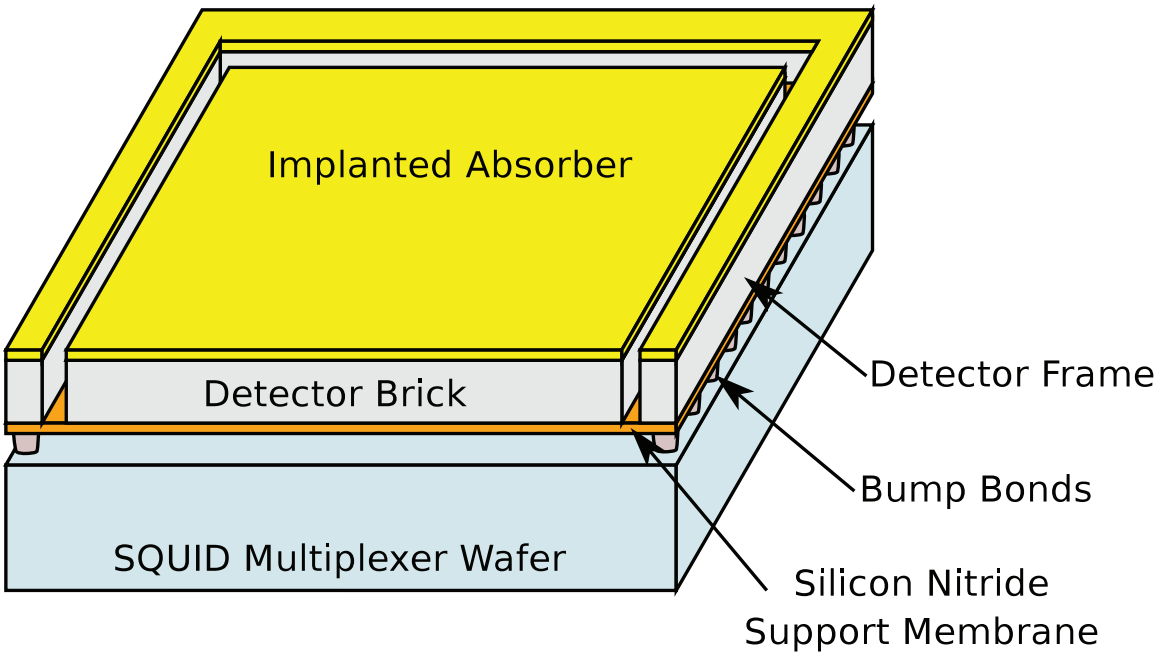

Figure 2.10: Schematic of a single TES pixel for the SCUBA-2 camera [32].

Three proposed CMB polarimeters: BICEP2, Keck, and Spider will also use TES arrays with different numbers of pixels [33]. Figure 2.11 shows an example of a dual-TES which is proposed for these instruments. This TES is composed of a Ti sensor with a T_c of ∼450 mK in series with an Al sensor with a T_c of ∼1 K. The Ti TES will be used in actual observations and the Al TES allows the laboratory testing over an increased dynamic range. Finally, researchers are now developing TES arrays of unprecedented sensitivity for the Background-Limited Infrared-Submillimeter Spectrograph (BLISS) (Figure 2.6) [18] and the SPICA Far-Infrared Instrument (SAFARI), which are two spectrometers proposed on the JAXA-ESA SPICA mission [34].

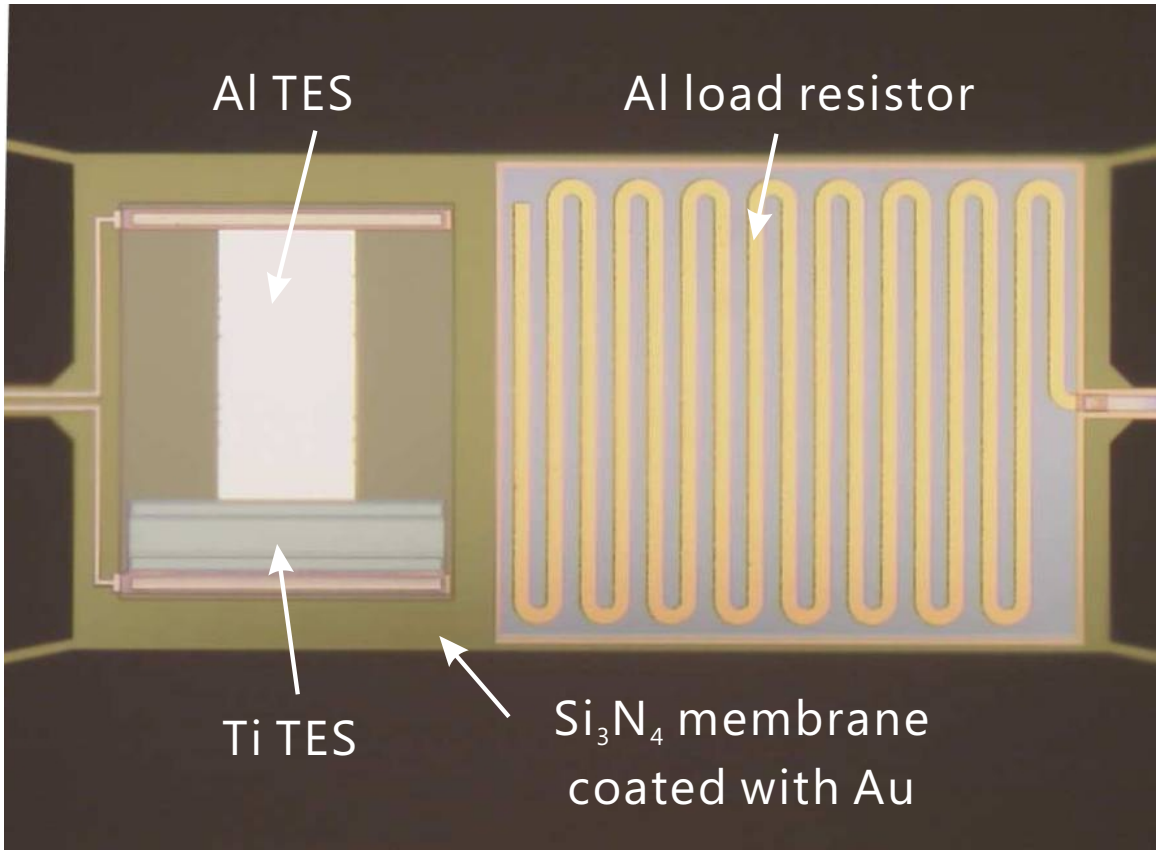

Figure 2.11: Micrograph of a dual-TES to be employed on BICEP2, Keck, and Spider [35].

Structural parameters and some important figures of merit of the TES devices mentioned above are summarized in Table 2.1.

Table 2.1: Summary of parameters of TES devices for astronomical missions.

Instrument	Sensor	Thermal Link	Absorber	Coupling Method	T_c (mK)	NEP ($W/\sqrt{Hz}$)
FIBRE [20]	Mo-Cu	Si membrane	Absorber coated on Si membrane	Quarter-wavelength resonant backshort	450	3×10^{-17}
MUSTANG [22]	Mo-Au	Si membrane	Bismuth coated on Si membrane	Free space	450	$\sim10^{-17}$
GISMO [36]	Mo-Au	Si membrane	Bismuth coated on Si membrane	Quarter-wavelength reflective backshort	460	4×10^{-17} [24]
APEX-SZ [25]	Al-Ti	Si_3N_4 spiderweb	Au on spiderweb	Feedhorn	450	$\sim10^{-16}$
MBAC [26]	Mo-Au	Si substrate	Ion-implanted Si substrate	Free space	512 [37]	4.1×10^{-17} [37]
SCUBA-2: 450μm wavelength [27]	Mo-Cu	Si_3N_4 membrane	Ion-implanted Si brick	Free space	194.8	1.12×10^{-16}
SCUBA-2: 850μm wavelength [27]	Mo-Cu	Si_3N_4 membrane	Ion-implanted Si brick	Free space	135	4.2×10^{-17}
BICEP2, Keck, and Spider [33]	Al and Ti dual sensor	Si_3N_4 membrane coated with Au	Au microstrip line	Antenna	450 (Ti)	$\sim10^{-17}$

Unless specified otherwise, data were quoted from references annotated in the 1^{st} row.

Chapter 3

Fabrication Process

In this chapter, the fabrication process of our TES devices is described. Most of the fabrication steps were conducted in the Nanofab of University of Alberta [38] by using standard microfabrication techniques. From designing the lithographic photomasks to manufacturing devices in the cleanroom, each step is presented in detail. Application notes and possible improvements are also summarized for future reference.

3.1 Process Flow

The first step in any microfabrication process is to develop a process flow. In this section, I summarize the fabrication process flow for the TES detectors, shown schematically in Figure 3.1. In steps 1 and 2 a niobium (Nb) layer is deposited on a silicon (Si) wafer, which has been pre-coated with 1 μm silicon nitride (Si_3N_4) on both sides. In step 3 the Nb superconducting sensors were patterned by what is known as the lift-off process. In step 4, thin layers of chromium (Cr) and gold (Au) were deposited on top of the Nb layer.

In step 5 wet etching of Au followed by Cr removes the elements everywhere except for the contact pads. In step 6 a layer of protective coating was spin-coated onto the front side of the wafer to protect the Nb sensors from the subsequent KOH etching. In step 7 Si_3N_4 on the back side of the wafer was etched using reactive ion etching (RIE) to expose the underlying bulk Si. In step 8 photoresist residues from step 7 were removed by an O_2 plasma. In step 9 the exposed bulk Si was etched away with a KOH solution, leaving the 1 μm thick Si_3N_4 membrane on the front side of wafer. In step 10 the protective coating from step 6 was stripped off. In step 11 a thin layer of Au was deposited on back side of the released Si_3N_4 membrane to act as an absorber. In step 12 aluminium (Al) wires were bonded to Au contact pads for connecting with external circuit. The completed wafers were returned to University of Lethbridge where they were diced and wire bonded to the external electronic circuitry in our cleanroom. Since the fabrication of the TES devices represents a major part of my thesis; the steps summarized above will be discussed in detail in the following sections.

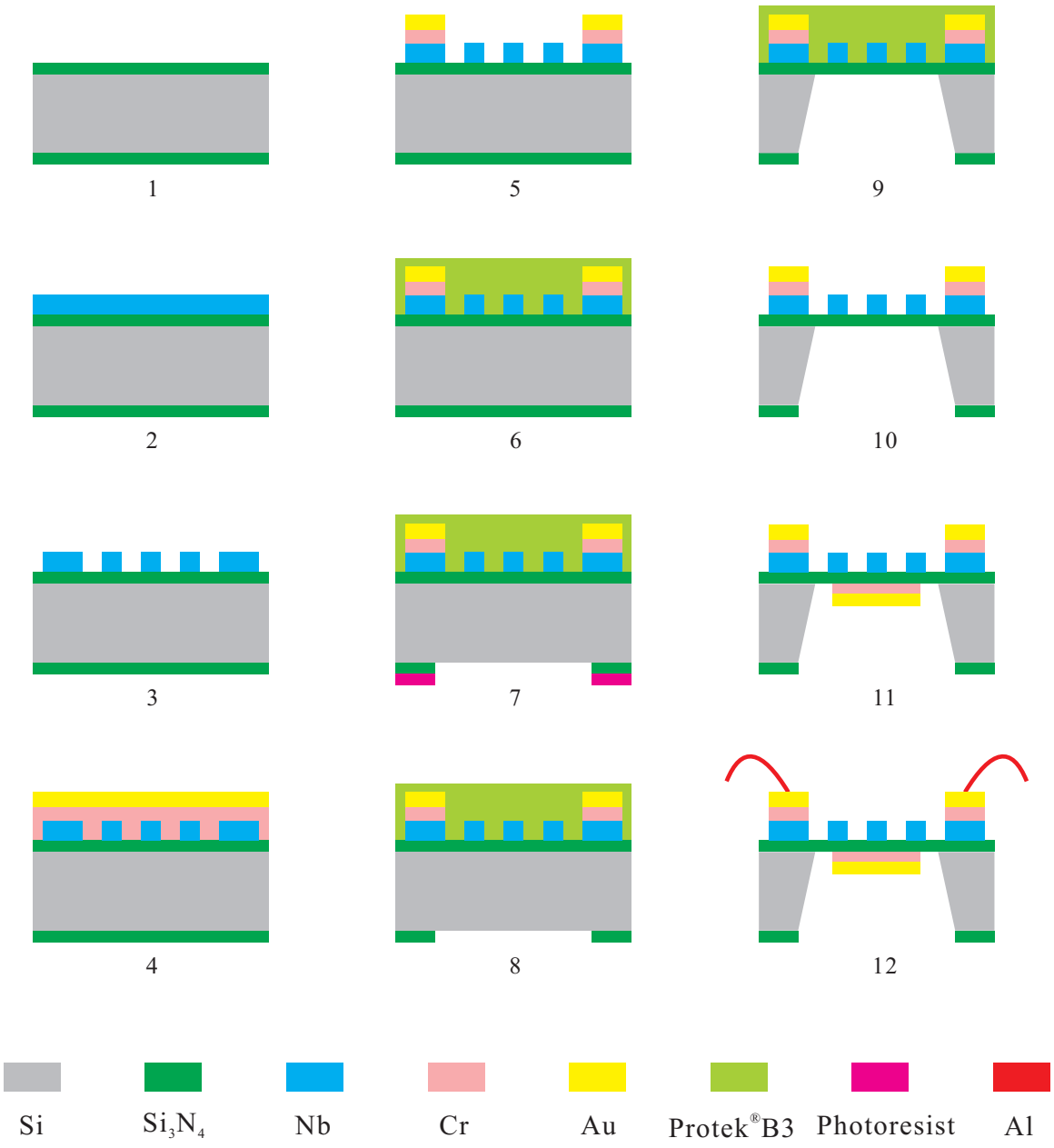

Figure 3.1: Process flow of the TES fabrication.

3.2 Silicon Wafer

Silicon wafers are commonly used as substrates for microfabrication due to their mechanical robustness and wide varieties. The Si wafers we used are of (100) crystal orientation, 100 mm diameter, 500 μm thickness, 1-10 Ω·cm resistivity, p-type, and prime grade [39]. All wafers have been pre-coated with 1 μm thick, low stress low-pressure chemical vapor deposition (LPCVD) silicon nitride on both sides (Figure 3.2). The low stress is important because in the final device the Nb detector is suspended on the fragile, 1 μm thick Si_3N_4 membrane. The primary flat shown in Figure 3.2 can be used to aligning wafer with microfabrication equipment, and the secondary flat indicates crystal orientation and doping type of the wafer; Figure 3.3 lists some common used wafers with flats.

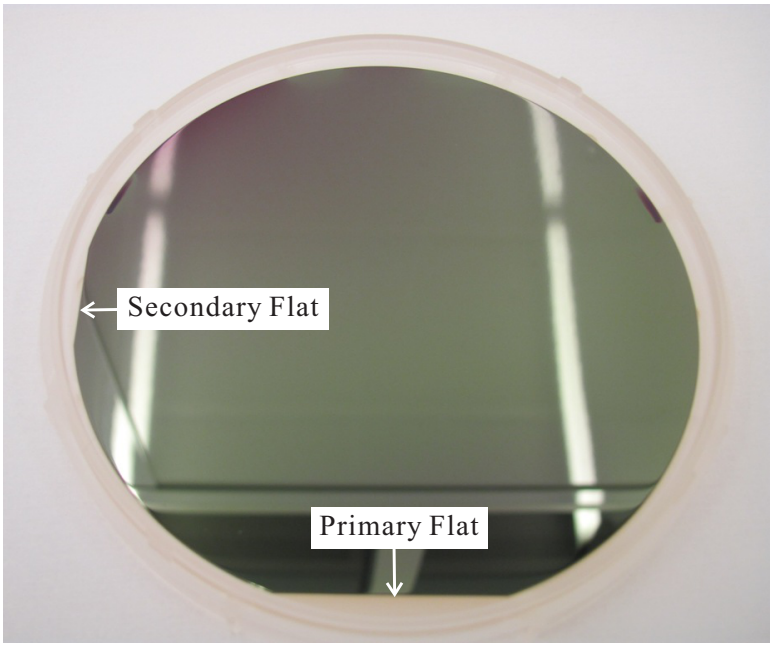

Figure 3.2: A Si wafer coated with 1 μm thick LPCVD silicon nitride on both sides.

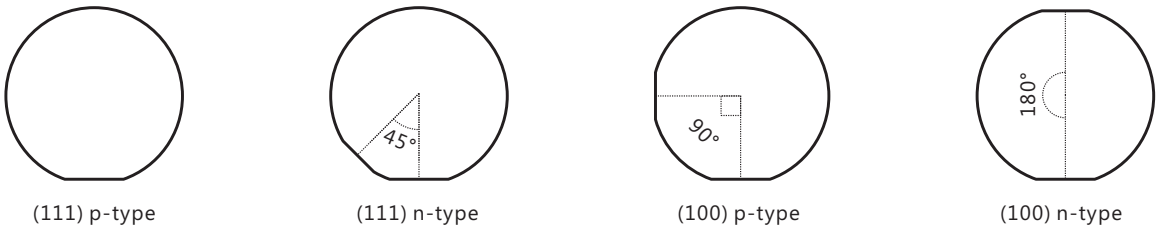

Figure 3.3: Wafer types and flats.

The etching of Si in alkaline etchants typically KOH (potassium hydroxide), which is anisotropic, meaning that the etch rate along different crystal planes of Si varies significantly. Figure 3.4 shows the three important crystal planes of a (100) Si wafer designated by their Miller indices. The wafer surface lies in the (100) plane, the primary flat lies along the (110) plane, and the angle between (100) and (111) planes is 54.7° [40]. When placed in KOH solution, the etch rate of the Si along the (100) planes is much higher than along the (111) planes. Therefore, a square window of exposed Si will be etched into inverted pyramid structures with the (111) planes as the sloped walls and the (100) plane as the bottom, as shown in Figure 3.4. If the size of the exposed Si window is small, as shown to the left in Figure 3.4, then the etching stops when the (111) planes meet to form a V-shape groove. This provides a method of designing scribe lines to make wafer dicing process easier. On the other hand, if the window is large enough, etching will continue until the Si_3N_4 membrane is reached, since Si_3N_4 is relatively insoluble in KOH compared to Si. This is the method we have used to release the Si_3N_4 membranes on the back side of the wafers. The details of this process is discussed in the following section.

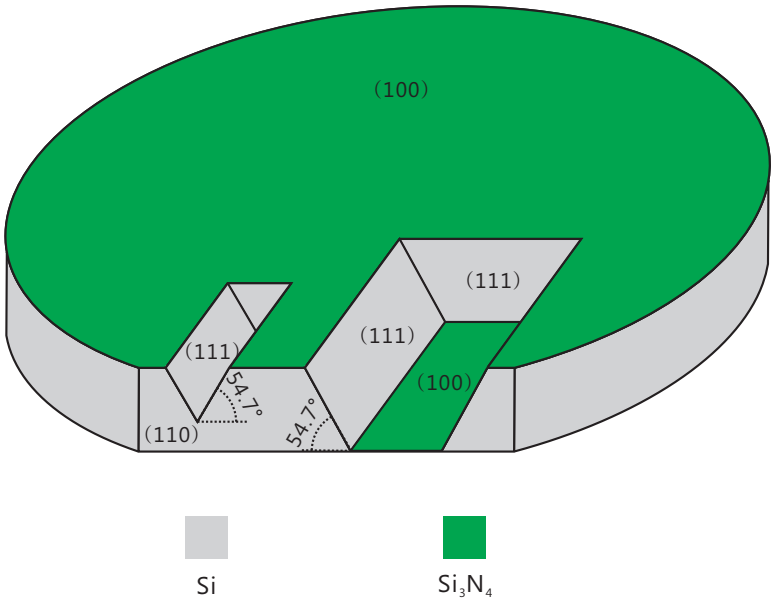

Figure 3.4: Illustration of the etching geometry of a (100) Si wafer.

3.3 Photomask Design

A crucial part of any microfabrication process is the design of photomasks, which are commonly used in photolithography to transfer designed patterns to substrates. A photomask usually consists of a piece of glass coated with chromium where some transparent windows exist. Light sources shine through these windows and expose the light-sensitive photoresist on the corresponding areas of a substrate so that patterns on the photomask are projected onto the substrate. A total of three photomasks are used for our fabrication: a Nb lift-off mask, a Au/Cr wet etch mask, and a back-side Si_3N_4 etch mask (Figure 3.5, 3.6, 3.7). The Nb lift-off mask is a negative (non-inverted) mask and the other two are positive (inverted) masks. I conducted the mask designing process in Nanofab; the writing of the

mask was conducted by Nanofab staff using the Heidelberg DWL 200 Pattern Generator [41].

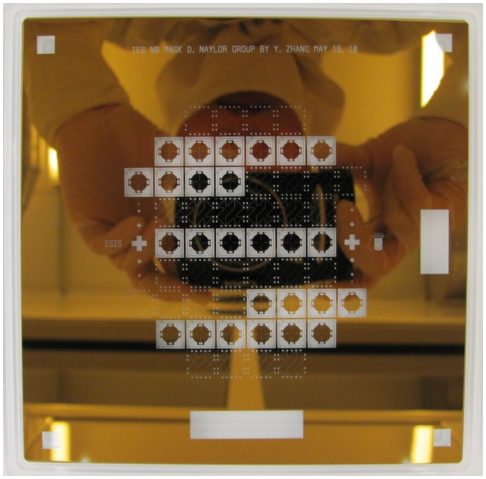

Figure 3.5: Nb lift-off mask.

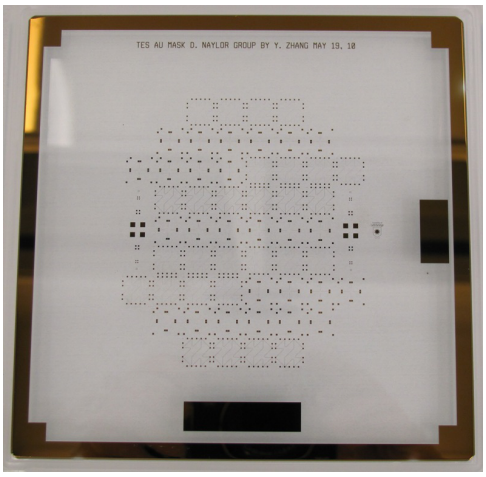

Figure 3.6: Au/Cr wet etch mask.

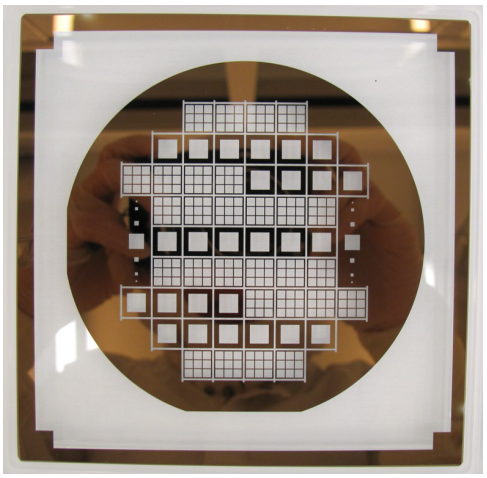

Figure 3.7: Back-side Si_3N_4 etch mask.

3.3.1 Mask Design Software

The graphical layout of all masks is designed using L-Edit software, one component of Tanner EDA [42], which is the default software available in University of Alberta's NanoFab facility. Other CAD software packages such as AutoCAD, however, can be used as long as they are capable of producing a GDSII formatted output file. L-Edit is adequate for standard mask design, however, for more complex geometrical patterns, such as spirals, MEMS Pro [43], with the extended Macros, is a better alternative.

3.3.2 Design Considerations

When designing masks for processes that involve several steps it is important to take into account potential alignment issues; in what is known as the edge margin (Figure 3.8). As a rule of thumb any pattern should avoid the outer 2-4 mm around edge of Si wafer in order to accommodate handling the wafer with tweezers. In our case, we require

the option of using the outer part of the wafer as part of an O-ring seal when using a specially designed apparatus for KOH etching.

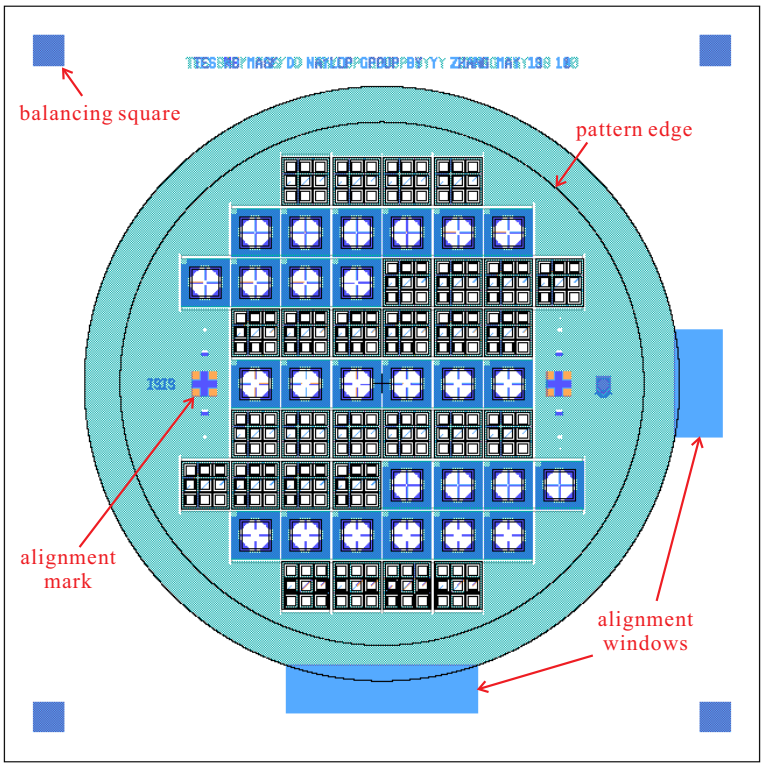

Figure 3.8: Three masks designed by L-Edit software lined up together.

After submitting the GDSII file produced by L-Edit for mask fabrication, the pattern generator will automatically center the design on a mask. For multi-layer alignment, all masks are forced to have the same center by placing balancing squares at four corners of each mask (Figure 3.8); this is known as mask centering.

Two alignment windows (Figure 3.8) are placed along the primary and secondary flats on the Nb lift-off mask and the Au/Cr wet etch mask. During lithography, these windows can be used as rough alignment references to the flats on the wafer. This is

especially useful for the negative Nb lift-off mask where most areas are covered by opaque chromium.

Since the viewing system on the mask aligner used to check the alignment of the mask and the wafer prior to lithography cannot observe the balancing squares, additional alignment marks are used (Figure 3.9); these alignment marks are extremely important for multi-layer alignment. The alignment marks consist of a set of features on masks which serve as fine alignment references to position patterns on different masks to the same wafer. Good alignment marks can make multi-layer lithography much easier, yet there is no defined best design for them. The shape and size of alignment marks may vary with many factors especially with lithography sequences.

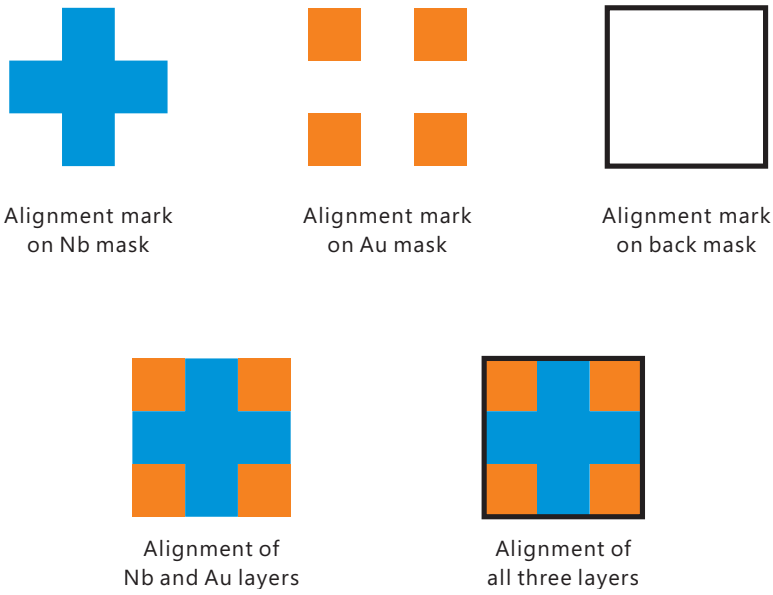

Figure 3.9: Alignment marks for each mask and mask overlapping after each lithography alignment.

The alignment marks for our Nb lift-off mask are a group of crosses, negative

crosses for the Au/Cr wet etch mask, and transparent windows for the Si_3N_4 etch mask. The overlapping of different alignment marks after each lithography alignment is shown in Figure 3.9. Among each set, the largest alignment mark is used for rapid aligning, and the smallest mark provides the best alignment resolution.

3.3.3 Si Etching Window

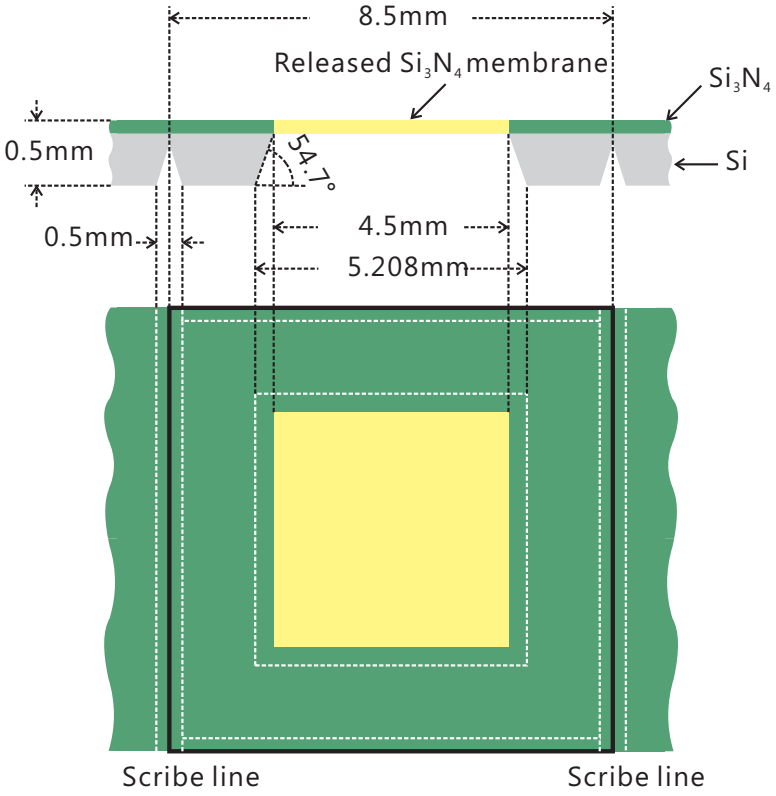

Figure 3.10: Cross-sectional view and top view of a Si_3N_4 etch window for a single-pixel device.

Achieving the desired size of the Si_3N_4 membrane using KOH etching of the Si substrate requires careful calculation. The size of the Si etch windows on back side of wafer (open windows on Si_3N_4 etch mask in Figure 3.7) can be calculated from the desired front-

side Si_3N_4 membrane size after KOH etching, the thickness of the wafer, and the 54.7° angle between the wafer surface (the (100) plane) and the (111) planes. For example, in the case of the 8.5 mm×8.5 mm single-pixel device, we want the front-side Si_3N_4 membrane to be 4.5 mm so that the calculated etch window on the mask is 5.208 mm. Scribe lines of 0.5 mm in width surround each device, and will be etched into V-shape grooves of depth the order of 300 μm. Figure 3.10 illustrates the schematic diagram of the Si_3N_4 etch window on the mask.

One limitation of the anisotropic wet etch which can be seen in Figure 3.10, is the fact that the 54.7° sloped walls inevitably take some room on the back side of the wafer, which sets a limit on how close the detectors can be packed together. In this regard, a thinner initial wafer is to be preferred, and in future fabrication we intend to use the 300 μm thick wafer.

3.4 Lift-off Technique

The lift-off technique to pattern Nb transition edge sensors was used instead of the more commonly-used method of fluorine-based plasma etch, as the latter is not available in NanoFab for safety concerns. Lift-off is a process to pattern metal with a sacrificial layer, usually photoresist. As shown schematically in Figure 3.11, the lithography process transfers the inverse pattern of interest to the photoresist on the wafer, followed by the metal layer deposition. Because the thickness of the metal layer is less than that of the photoresist, by immersing the wafer in solvent the metal on top of the photoresist is washed away together with dissolved photoresist, while metal in direct contact with the wafer remains [40].

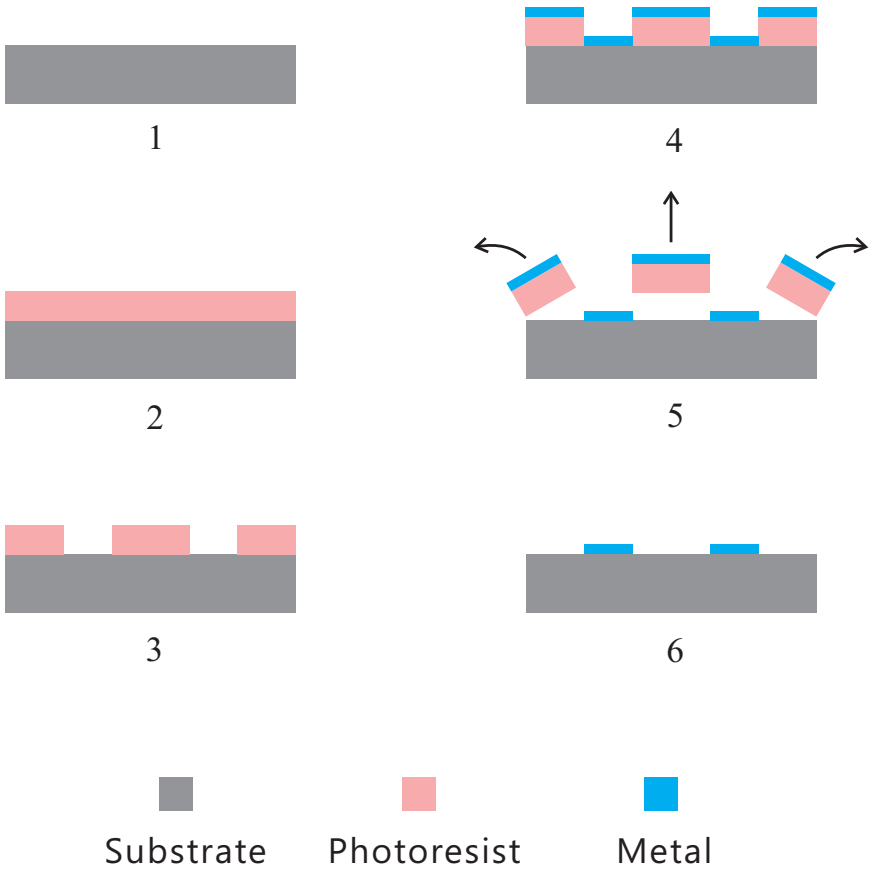

Figure 3.11: Schematic of the lift-off technique.

3.4.1 Photoresist Coating

Prior to photoresist coating, two steps should not be neglected. The first is to mark each wafer with a number using a scratch pen for future reference; the second is to blow the wafer surface with a clean air gun to remove dirt and particles.

The first step in the applying the photoresist coating is to spin-coat a layer of HDMS (hexamethyldisilazane) on the wafers to promote adhesion of photoresist to silicon nitride. This step takes 17 min in a vacuum bake/vapor prime oven [44] (Figure 3.12) with

an automated program.

Figure 3.12: The vacuum bake/vapor prime (HMDS) oven.

The photoresist, HPR 504 [45], was used in all lithography procedures including lift-off, Au/Cr wet etch, and Si_3N_4 plasma etch. The recipe is 5-10 mL of HPR 504/per wafer, initially spinning at 500 rpm for 10 seconds, then at 4000 rpm for 40 seconds, followed by a soft-bake at 115°C for 90 seconds. Detailed procedures and notes are listed in the steps below.

1. Pour enough HPR 504 into a clean small beaker, cover the beaker with a large beaker to prevent evaporation (if the photoresist has recently been taken from a refrigerator it must be allowed to rest for 30 minutes to eliminate bubbles).

2. Clean the vacuum tip of the spinner [46] (Figure 3.13) with a clean room wipe and acetone.

Figure 3.13: Spinner.

3. Choose an ideal chuck that is a little bit smaller than the wafer, and clean it with a clean room wipe and acetone. Place the chuck onto the spinner by lining up its slots to the bars of spinner. It should feel like pushing on the chuck in two steps.

4. Use a test wafer to set spin and spread parameters as the recipe.

5. Center the wafer onto the chuck, be very careful do not scratch the wafer surface, and then press the vacuum button. The wafer should be held tight, if not the

vacuum tip needs be cleaned or the chuck needs to be changed.

6. After one wafer is finished spinning, it is placed on a vacuum hotplate [46] (Figure 3.14) for the baking cycle.

Figure 3.14: Vacuum hotplate.

7. After baking, the wafers are placed on a clean room wipe, near the mask aligner in baking sequence. The lithography process can start after 15 minutes when the wafers have reached equilibrium.

3.4.2 Lithography

The lithography process uses an ABM infrared mask aligner [47] (Figure 3.15) to transfer patterns on the masks to the wafers. It takes ∼30 min for the light source to stabilize after turning on the aligner, so HMDS and photoresist coating can be done during this time. As discussed above, a total of three lithography processes are involved in the

fabrication flow. These steps are summarized in the following section.

Figure 3.15: ABM infrared mask aligner.

1. Set the expose time on the mask aligner to 3.2 s.

2. Blow both sides of the mask with the filtered nitrogen gun to remove dirt and particles.

3. Check if the appropriate chuck and mask frame are chosen for the wafer.

4. Mount the mask on the mask frame with chromium (brown color) side facing down. Turn on the mask frame vacuum switch (Figure 3.16) to immobilize the mask and the frame.

5. Lift the mask frame up. Place the wafer on the wafer chuck. Turn on the substrate vacuum switch to hold the wafer still.

6. Using the alignment windows on the mask as references to flats on the wafer (Figure 3.8), lower the mask frame and roughly align the wafer with the mask.

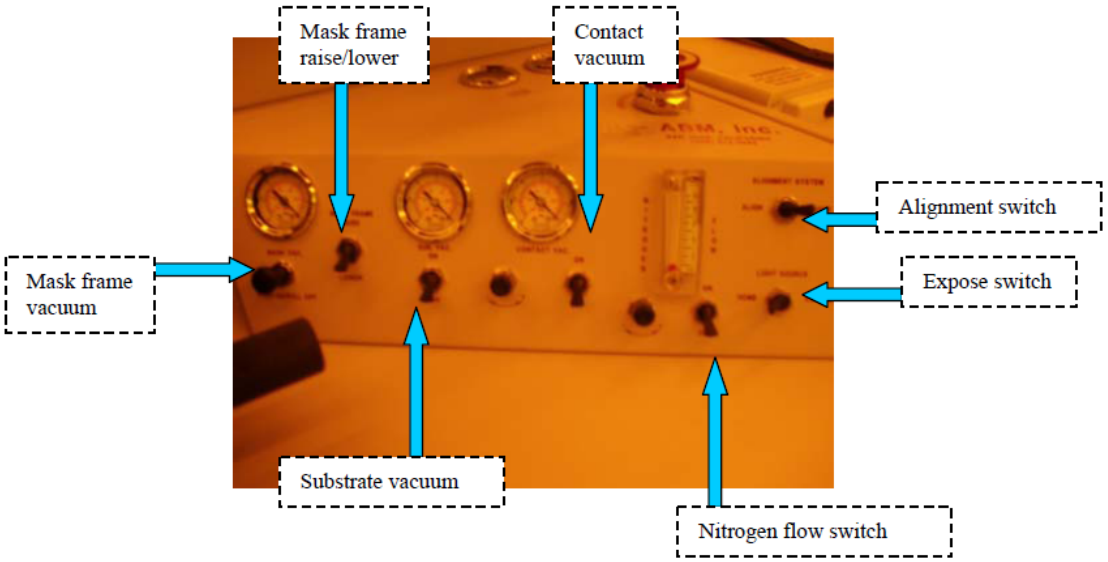

Figure 3.16: Operational switches on the aligner.

7. Turn on the nitrogen flow switch.

8. Lift the wafer to bring it close to the mask by turn the large adjustment knob (Figure 3.17) counter-clockwise. While doing this, press and hold the self leveling button to avoid the wafer substrate directly touching the mask.

9. Use the X, Y and Theta dials to align mask to the wafer. For the second (Au/Cr wet etch) and the third (Si_3N_4 etch) lithography alignments the microscope viewing system must be used together with alignment masks of decreasing sizes to ensure the different layers in the process flow are accurately registered. For the third alignment, infrared light probes are needed to see through the wafer.

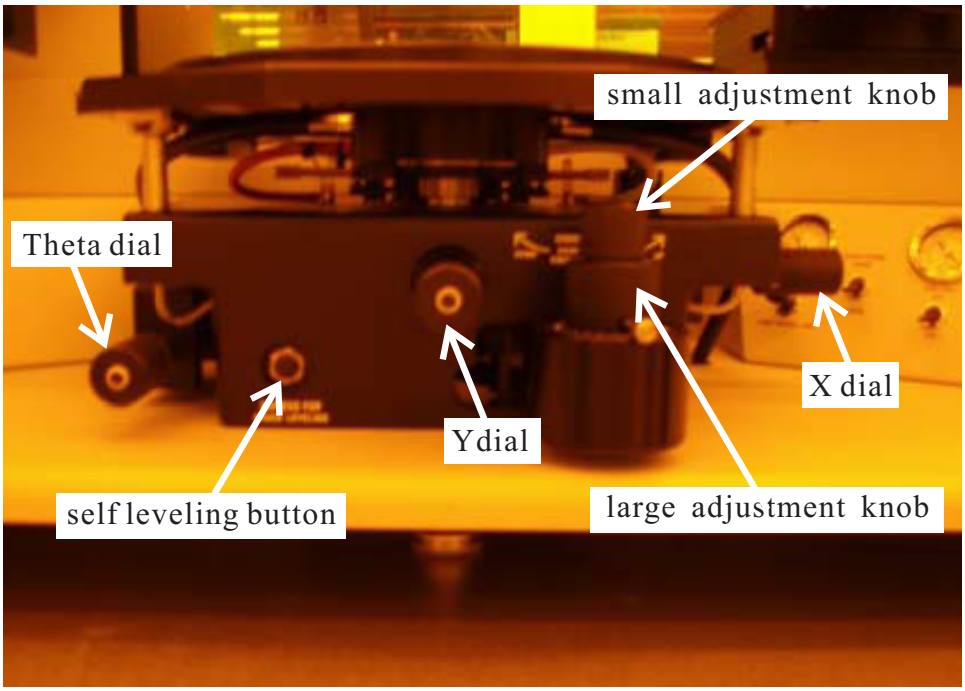

Figure 3.17: Alignment knobs on the aligner.

10. Once the system is aligned, the expose switch (Figure 3.16) is turned on. At this point, the exposed photoresist is activated.

11. When the exposure is complete, the wafer is removed from the mask aligner and immersed into the prepared 354 developer for approximately 15∼20 s, and washed with deionized (DI) water.

3.4.3 Nb Deposition

Since one goal of this thesis was to investigate of the variation of the transition temperature T_c with Nb thickness, Nb layers of thicknesses ranging from 10 to 100 nm were deposited onto the Si_3N_4 surface of the wafer (Figure 3.18) using the Floyd DC planar

magnetron sputtering system [48] (Figure 3.19). The system uses argon as the sputtering gas. Since the sputtering pressure is known to play an important role in the properties of the deposited Nb film (for example stress, density, resistivity, and transition temperature), two groups of wafers were processed at two argon pressures, 0.8 mTorr and 7 mTorr, respectively. The required Nb film thicknesses were determined from the sputtering rate, which are 12.5 nm/min for 0.8 mTorr pressure and 14.5 nm/min for 7 mTorr pressure, respectively. The performance of the detectors produced via the two argon sputtering pressures are presented in Chapter 6.

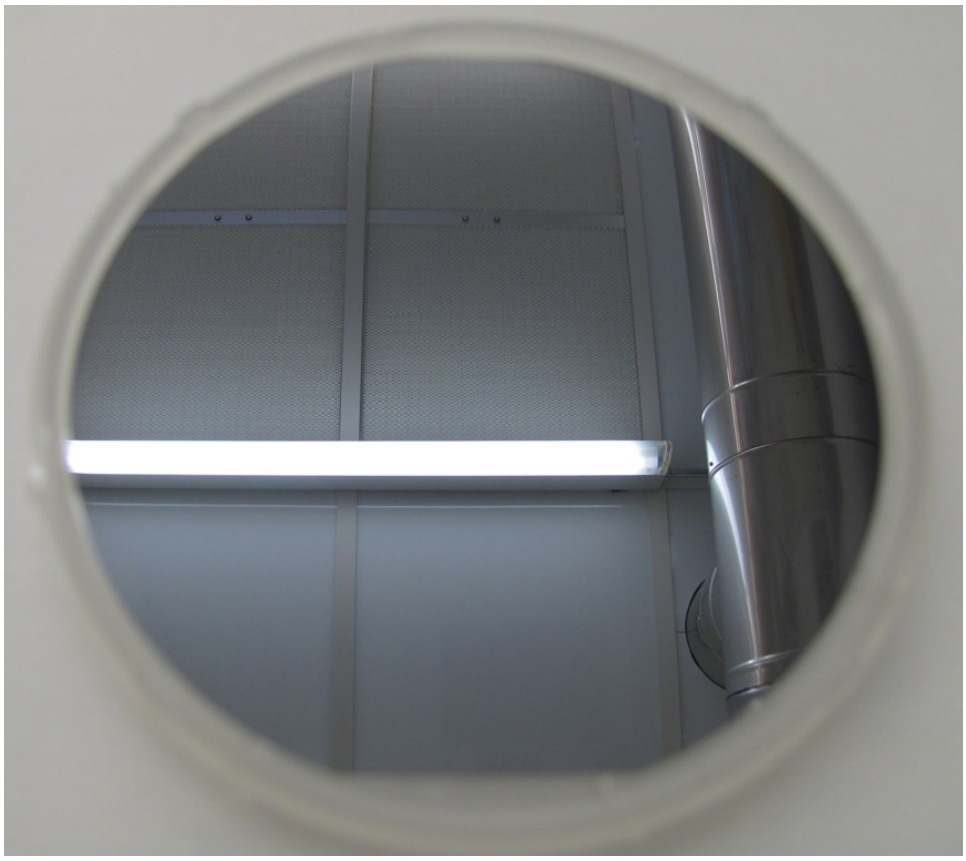

Figure 3.18: A Si wafer deposited with a layer of Nb film.

Figure 3.19: Floyd sputtering system.

3.4.4 Lift-off

The lift-off process took place by immersing the wafers in an ultrasonic tank filled with acetone as shown in Figure 3.20. The arrow indicates the Nb fragments peeling off during the lift-off process. The use of an ultrasonic tank can expedite the process. The microscope pictures of the clean edges and sharp tips of devices in Figure 3.21 show the quality of the final device.

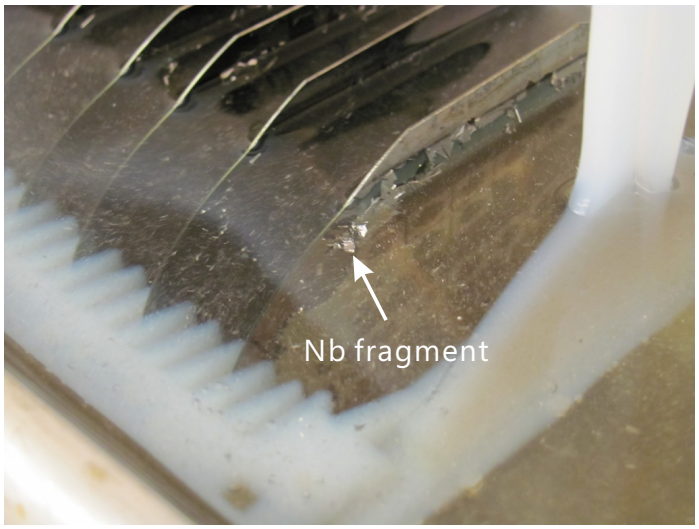

Figure 3.20: Lift-off in progress.

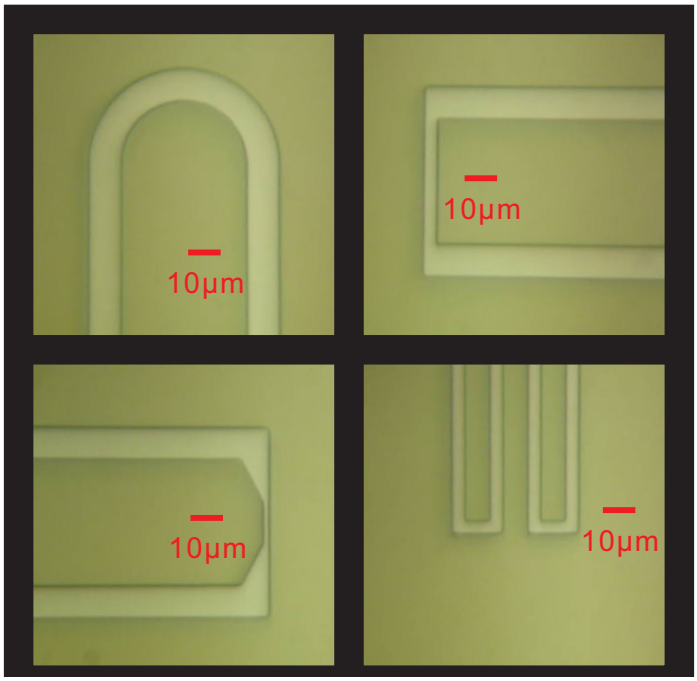

Figure 3.21: Lift-off results under microscope.

3.5 Cr/Au Deposition

In the next step Au contact pads were fabricated on the device to allow wirebonding to the external electronics in the final assembly stage. Before the Au can be deposited, a 50 nm layer of Cr is put down which works as an adhesion layer between Au and Nb. The Au layer was 150 nm thick for easier wirebonding. Both the Cr and Au were deposited using another DC planar magnetron sputtering system called Bob [48] (Figure 3.22). Bob allows both metals to be deposited in the same chamber without breaking the vacuum, which avoids a natural-oxide layer growing on the first-deposited metal. Table 3.1 shows sputtering parameters for the two metals. As before, the sputtering time can be calculated knowing sputtering rate and required film thickness.

Figure 3.22: Bob sputtering system.

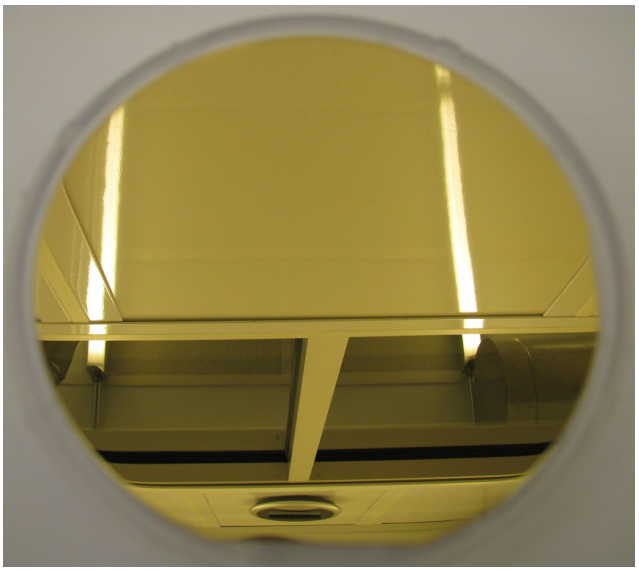

Figure 3.23: Wafer deposited with Cr and Au.

Table 3.1: Cr/Au sputtering parameters in the Bob system.

Metal	DC Power (W)	Sputtering Rate (nm/min)
Cr	300	9.1
Au	75	7.6

3.6 Au/Cr Etch

After the second optical lithography with the Au/Cr wet etch mask, Au and Cr wet etching were implemented in sequence to define the Au contact pads. Both the Au and Cr etchants are premade solutions; the former contains potassium iodide, iodine, and water, the later contains ceric ammonium nitrate, nitric acid, and water. The etch time is ∼45 s for Au and ∼35 s for Cr. The endpoint of both processes is monitored visually. Figure 3.24 shows the wafer at the beginning and ending of the etch process. As before, the process

can be expedited by continuous agitation. Since the Au etchant has a very dark color, it is important to keep monitoring the state of etching by holding wafer with tweezers, which can also accelerate the etching process. When the etch processes finish, wafers were washed with not only DI water but also acetone, so that photoresist residues can be removed to avoid contamination to the following protective coating step.

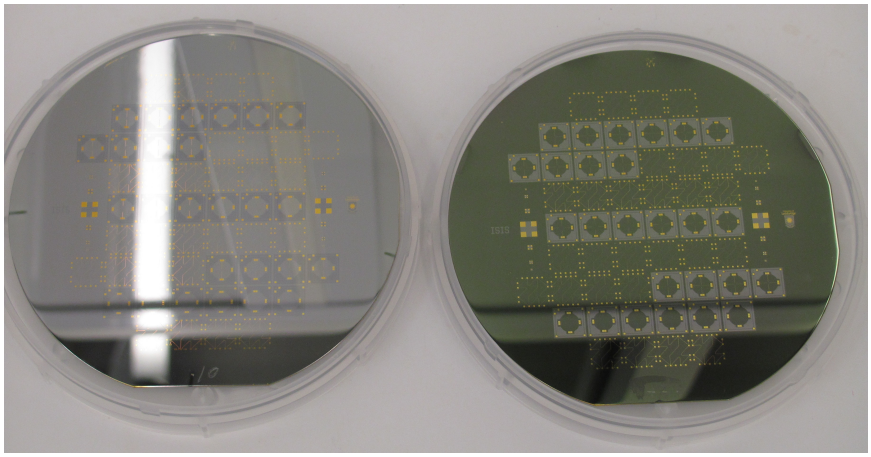

Figure 3.24: Comparison of wafer after Au etch (left) and Cr etch (right).

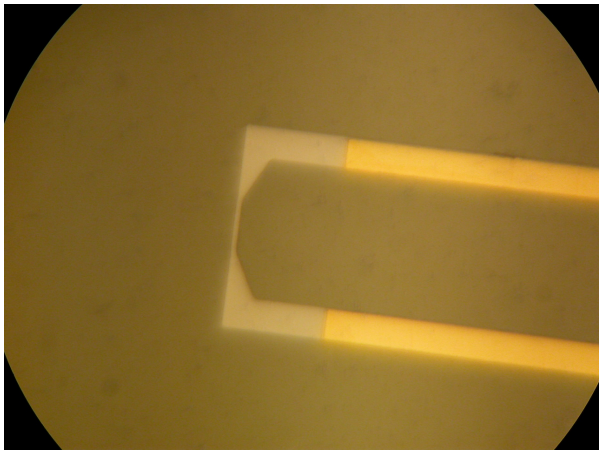

Figure 3.25: Microphotography of the Au/Cr etch result.

3.7 ProTEK® B3 Coating

In order to protect the Nb films from the following KOH etching, a layer of protective material, ProTEK® B3 [49], must be first coated on the front side of the wafer to protect the delicate devices. The process flow involves coating the device side of the wafer with ProTEK® B3 Primer and ProTEK® B3, the former is used to promote adhesion of the latter. The detailed steps are as follows:

1. ProTEK® B3 Primer Coating: spin-apply ProTEK® B3 Primer at 1500 rpm (accelerate at 10000 rpm/s) for 60 s; bake on hotplate at 205°C for 60 s.

2. ProTEK® B3 Coating: spin-apply ProTEK® B3 at 1000-4000 rpm (accelerate at >5000 rpm/s) for 60 s; bake on hotplate at 140°C for 120 s, and then at 205°C for 60 s.

The spinning process uses a Headway resist spinner [50] shown in Figure 3.26. Figure 3.27 shows the wafer after spin-coating and baking.

Figure 3.26: Headway resist spinner.

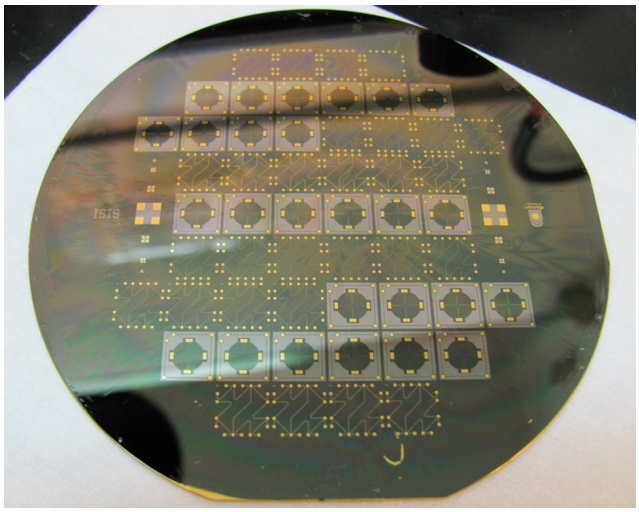

Figure 3.27: Wafer after ProTEK® B3 coating and baking.

3.8 Back Side Si_3N_4 Etch

The third lithography step is to open up windows with the Si_3N_4 etch mask on the back side of the wafer to remove the bulk Si. Once the image of the mask has been transferred, a reactive ion etch (RIE) etched away Si_3N_4 on the back side of the wafer (Figure 3.28). A fluoride based STS RIE system [51] (Figure 3.29) took about 4 minutes to etch the 1 μm thick Si_3N_4, which means that the actual etching rate was less than the theoretical etching rate of 7 nm/s. The reason might be that the theoretical etching rate is for PECVD (plasma-enhanced chemical vapor deposition) Si_3N_4, yet our wafers were deposited with LPCVD (low-pressure chemical vapor deposition) Si_3N_4. Since the reactants are hazardous, the operational procedure for this step is automated by software. The steps include:

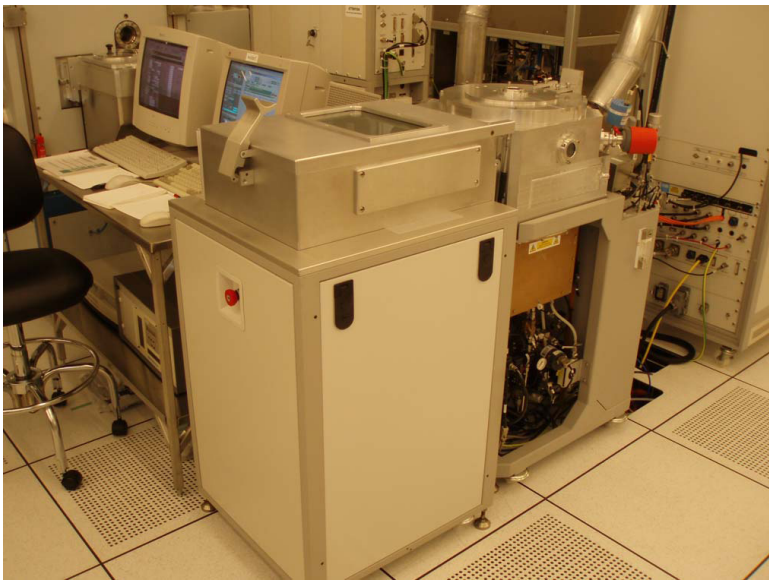

Figure 3.28: SIS RIE system.

1. Vent the system to air pressure.

2. Put the wafer to be etched and a bare, piranha cleaned wafer into the chamber, while the latter is for the following O_2 cleaning step.

3. Pump the system to $<$ 80 mTorr.

4. Load the O_2 clean wafer first and clean the chamber for 10 min with the O_2 clean recipe in the control software.

5. Unload the O_2 clean wafer and load the the wafer to be etched. Select the silicon nitride etch recipe and set etch time to 4 min.

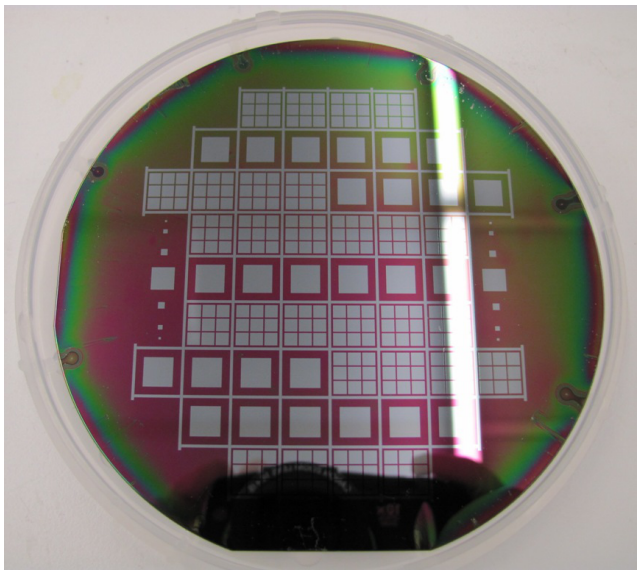

Figure 3.29: Back side view of wafer after Si_3N_4 etch. The shiny squares are exposed Si, and the red looking areas are photoresist.

3.9 Photoresist Ashing

Photoresist residues from the third lithography step (Figure 3.29) will interfere the following KOH etch and must removed. However, the previous plasma etch process causes damage to the photoresist so that the photoresist can no longer be removed simply with acetone [40]. An O_2 plasma was then used to ash photoresist in a μEtch RIE system (Figure 3.30). The recipe is listed below:

1. Prior to photoresist ashing, the system needs to be cleaned with an O_2 plasma of 80% O_2 flow at 150 mTorr for 10 min, with RF power of 220 W.

2. The photoresist ashing uses an O_2 plasma of 100% O_2 flow at 400 mTorr for 5 min, with RF power of 100 W.

The result of the photoresist ashing is shown in Figure 3.31. One concern of this

process was that the exposure to O_2 plasma may result in Nb oxidation, which will render the Nb non-superconducting.

Figure 3.30: The μEtch RIE system.

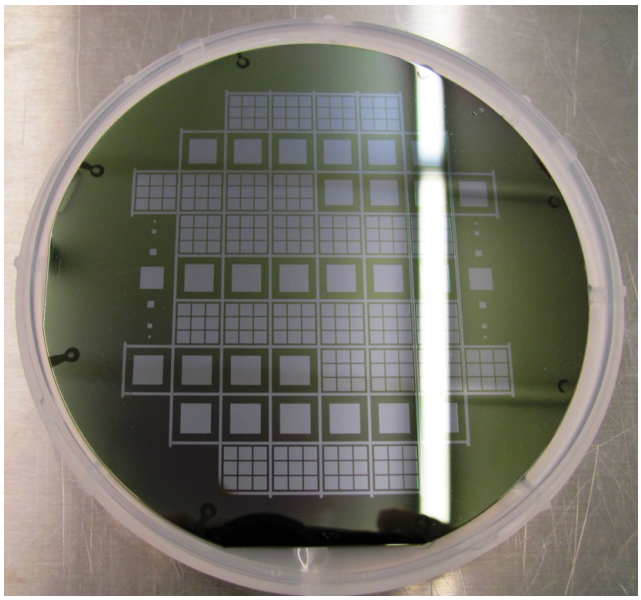

Figure 3.31: Back side view of wafer after photoresist ashing (see comparison with Figure 3.26).

3.10 Si Wet Etch with KOH

With the bulk Si exposed on the back side of the wafer it is etched away with a 40% KOH solution at 85°C. This is a relatively slow process that takes 7-8 hours to etch through the 500 μm thick bulk Si. We have experimented with two approaches; in one, conducted in NanoFab, wafers were coated with ProTEK® B3 and then were immersed in KOH tank inside the KOH fumehood (Figure 3.32). Experimental results show that ProTEK® B3 is a promising candidate, as it has the advantages that multiple wafers can be etched simultaneously, and most areas of the wafer can survive in the ∼8 hours of hot alkaline etching except for a small region around the edge. Figure 3.33 shows a resulting wafer after KOH etching using ProTEK® B3.

Figure 3.32: The KOH fumehood.

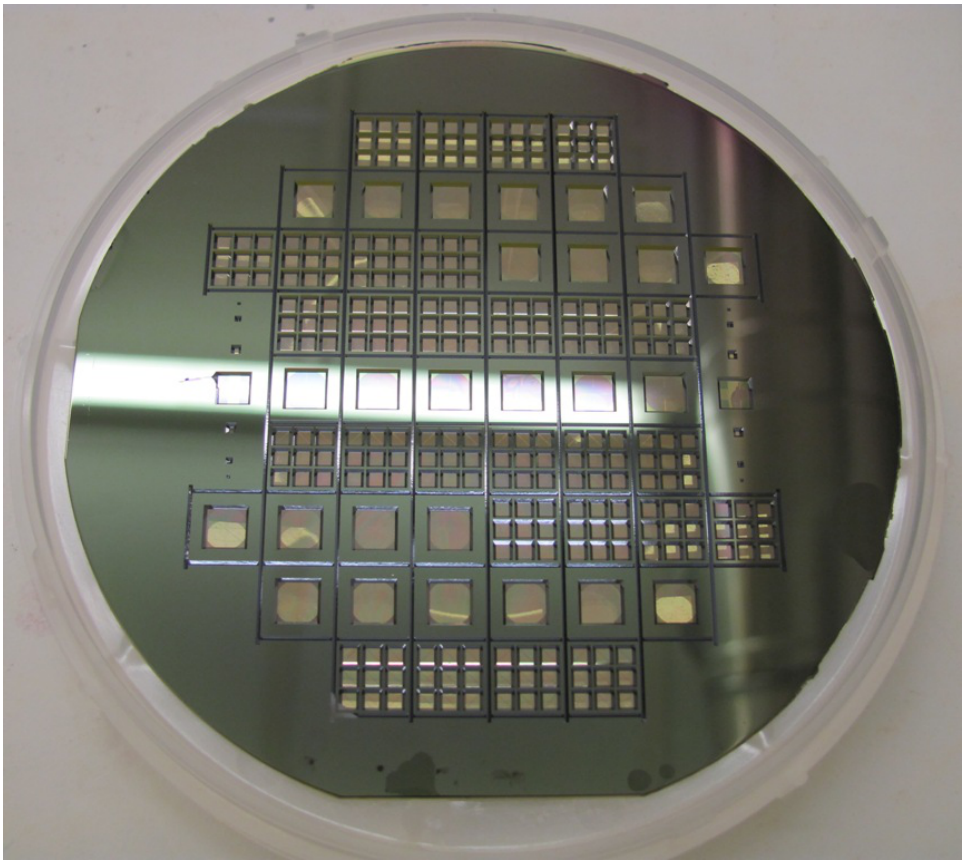

Figure 3.33: Wafer after Si etching. The transparent windows are release Si_3N_4 membranes of 1μm thick.

In the second method we designed a Teflon® [52] etch boat (Figure 3.34) in our laboratory at University of Lethbridge. Teflon® is insoluble in KOH. When the wafer was placed face down in the boat, the surface was sealed by an O-ring. The sealed front side includes a vent hole and stainless steel snorkel to allow for pressure equalization between front and back sides of the wafer [53] when the unit was immersed in the tank of KOH. This method was proved to be inexpensive and effective. It has the disadvantages, however, only allowing one wafer to be processed at a time, and should the wafer fracture during the etching process all the devices will be lost. By comparison, if a fracture occurred on a

ProTEK® B3 coated wafer, many devices will survive.

Figure 3.34: The Teflon® etch boat loaded with a wafer.

3.11 Removing ProTEK® B3 Coating

After the etching has completed, which can be determined from visual inspection of the wafer, the wafer is washed with DI water and then immersed in ProTEK® Remover 100 bath to strip off the ProTEK® B3 coating. In step 1 the wafer is immersed into the first ProTEK® Remover 100 bath at room temperature for 20 min. In step 2 the wafer is transferred into the second ProTEK® Remover 100 bath at room temperature and soaked for 20 min. In step 3 the wafer is rinsed with IPA (isopropyl alcohol) for 5 min, DI water for 2 min, and then dried by air gun blow. Our experiments show that the ProTEK® Remover 100 can be replaced with acetone.

One disadvantage of using the ProTEK® is that a residue may be left on the wafer. As a result, we chose to use an O_2 plasma strip process with the μEtch RIE system following the wet strip process and the recipe is: 50 sccm (standard cubic centimeters per minute) O_2 flow at 50 mTorr for 20 s, with RF power of 300 W. However, it also has the possibility of Nb oxidation.

3.12 Cr/Au Absorber Deposition

With the Si_3N_4 membrane now released, Cr/Au absorbers were deposited directly onto the surfaces using a homemade Al shadow mask [53]. The shadow mask shown in Figure 3.35 consists of small apertures which define the area of the Au absorbers to be deposited. The required absorber sizes are: 3 mm in diameter for the single-pixel devices and 1 mm in diameter for the 3× multi-pixel devices. Once cleaned, the the shadow mask is aligned to a wafer with all apertures centered with corresponding membranes, and then clamped to keep the wafer from displacing during transferring into the deposition system. Alignment is the most critical step of absorber deposition, as at this stage wafers are so fragile that careless handling could easily damage them. The screws should be just loose enough to keep the wafer from moving but not to transform shape of the mask and crack the wafer. Since alignment is done with visual inspection the accuracy is not perfect but still acceptable. Further accuracy improvements can be achieved by fine machining of the shadow masks.

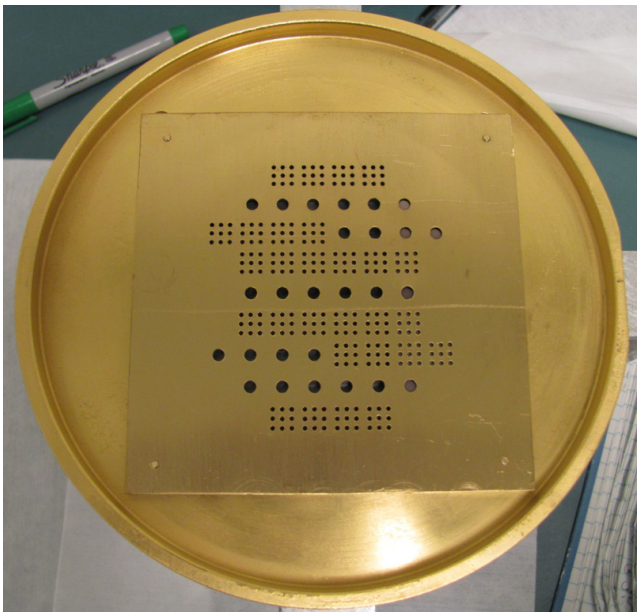

Figure 3.35: A shadow mask.

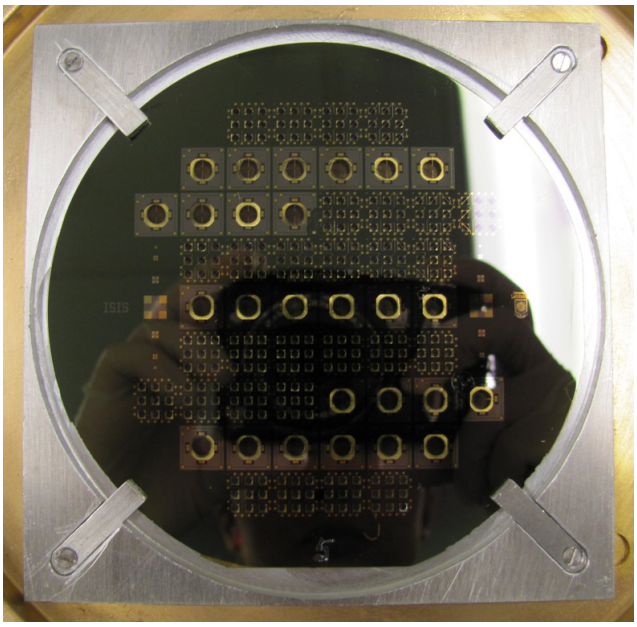

Figure 3.36: A Wafer fixed in a shadow mask via screws and small Al plates.

The deposition process took place in the Floyd sputtering system. The optimum absorption of radiation at sub-millimeter wavelength is a function of the Au thickness. Following recommendations by Professor Peter Ade [54], a layer of 20 nm thick Cr (adhesion layer) and a layer of 20 nm thick Au (absorber layer) were deposited in sequence in the same vacuum chamber as discussed above. Table 3.2 lists the major deposition parameters.

Table 3.2: Cr/Au sputtering parameters in the Floyd system.

Metal	DC Power (W)	Sputtering Rate (nm/min)	Argon Pressure (mTorr)
Cr	75	23	7
Au	80	14.2	7

3.13 Al Wire Bonding

After absorber deposition, the wafers are returned to our laboratory at University of Lethbridge where they are easily diced into separate devices using the scribe lines as shown in Figure 3.37. We manually separate devices by applying slight pressure along scribe lines instead of using a dicing saw. In the final step, a diced device is glued onto a IPA cleaned 12-pin TO8 header [55] (Figure 3.38), and a K&S wire bonder [56] is used to bond the Au pads from the device to pins of the TO8 header. The bonding process and results are shown in Figure 3.39 and Figure 3.40. The device then is covered with a cap for protection, and device number is marked on the cap for testing reference.

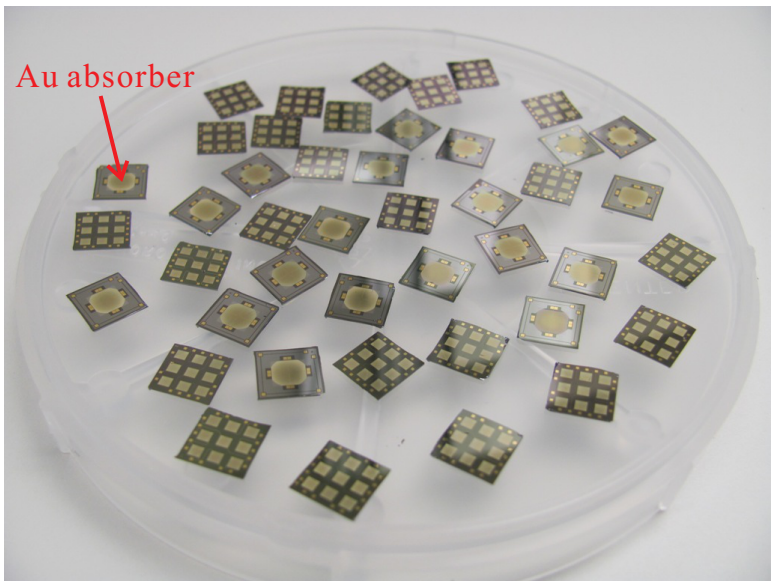

Figure 3.37: Diced devices.

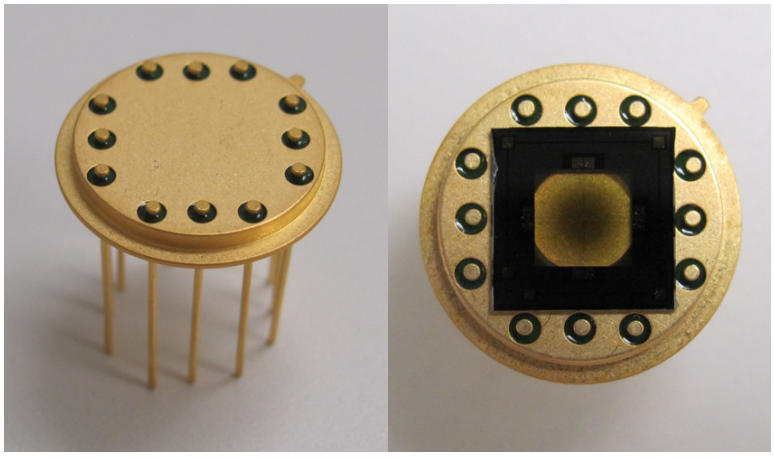

Figure 3.38: A diced device is glued onto a 12-pin TO8 header.

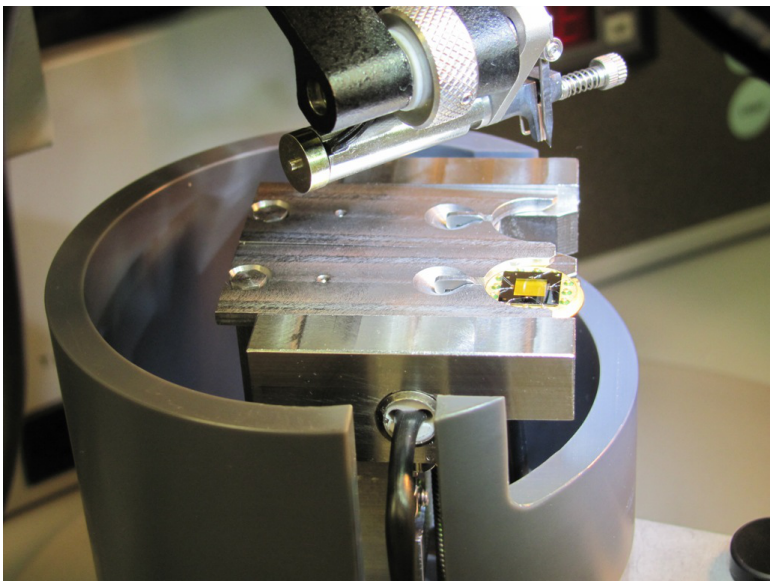

Figure 3.39: Wire bonding in progress.

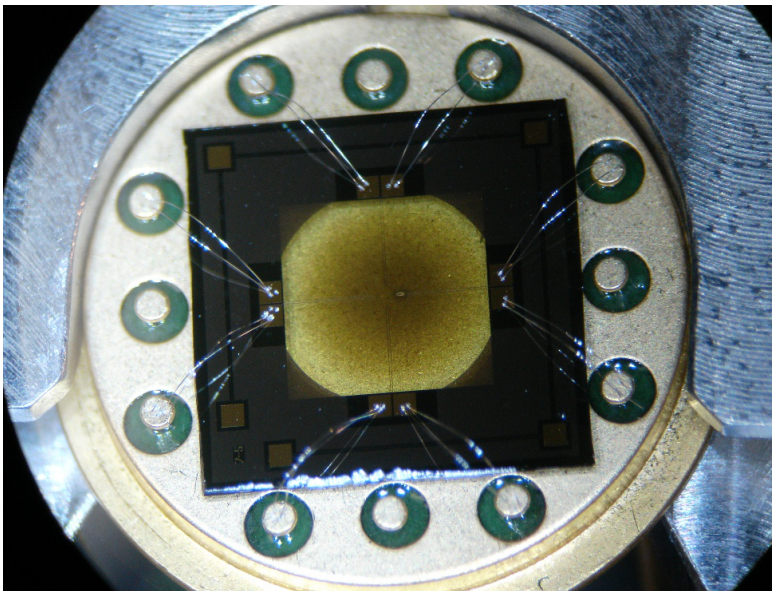

Figure 3.40: A device bonded with Al wires.

3.14 Summary and Possible Improvements

We have successfully developed a repeatable process flow to fabricate high quality TES detectors. Some suggestions for improvements in design and fabrication are listed below:

1. Because of safety issues in using fluorine based plasma to etch Nb, we used the lift-off method to pattern Nb sensors. Although lift-off has produced very good results, it would still be useful to try plasma etch and then compare the effect of the two methods in future, because in plasma etching all three metals (Nb, Cr, and Au) can be deposited in a single vacuum step, but for lift-off the deposition is discontinuous, which could grow natural oxidation on Nb films and therefore affect Nb sensor properties.

2. In order to reduce the wasted space caused by the 54.7° etching angle, and to allow fabrication of more devices on a single wafer, thinner wafers should replace the current 500 μm wafer. This will also greatly shorten Si etching time.

The design and fabrication process described in this chapter could not have been done without the access to University of Alberta's Nanofab laboratory, we are especially grateful for the director Dr. Ken Westra and all the staff, especially Stephanie Bozic and Les Schowalter for their kindly supports and valuable suggestions. I'd also like to thank for CMC Microsystems for financial support of both fabrication and traveling.

Chapter 4

Cryostat

In order to operate TES detectors at their transition temperatures, which range between 4 and 9 K, a VeriCold He7 system [57] is used as the cryostat. The two main components of the system, a pulse tube cooler and a two-stage ^{3}He/^{4}He sorption pumped refrigerator [58], are mounted in an evacuated dewar (Figure 4.1 and 4.2). The pulse tube cooler works as the primary cooling unit, and the refrigerator as the secondary, lower temperature cooler which cools the detectors to their operating temperature. There are also other necessary accessories associated with the dewar. Figure 4.3 shows how these components are connected. The step-by-step process from preparing of a detector to installing and measuring its performance will be discussed in Chapter 5. In this chapter we will focus on the operating principles of the system.

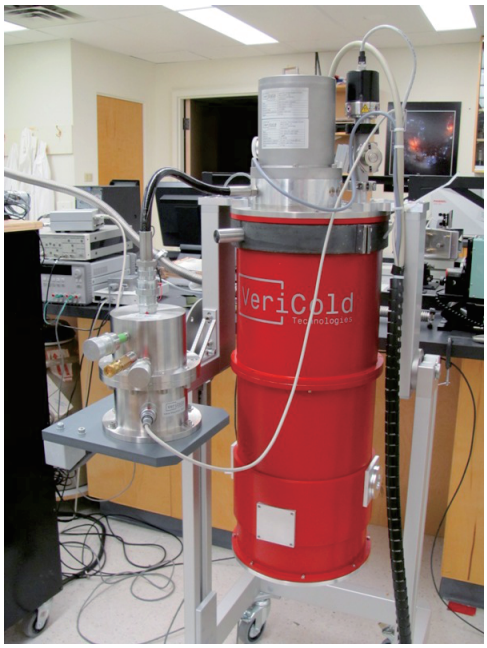

Figure 4.1: Photograph of the VeriCold He7 cryostat.

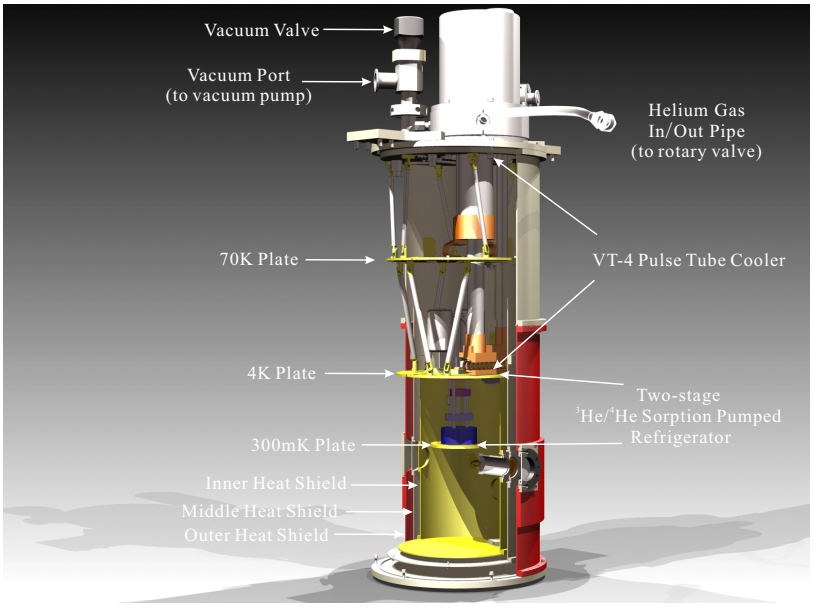

Figure 4.2: CAD visualization of the VeriCold He7 cryostat.

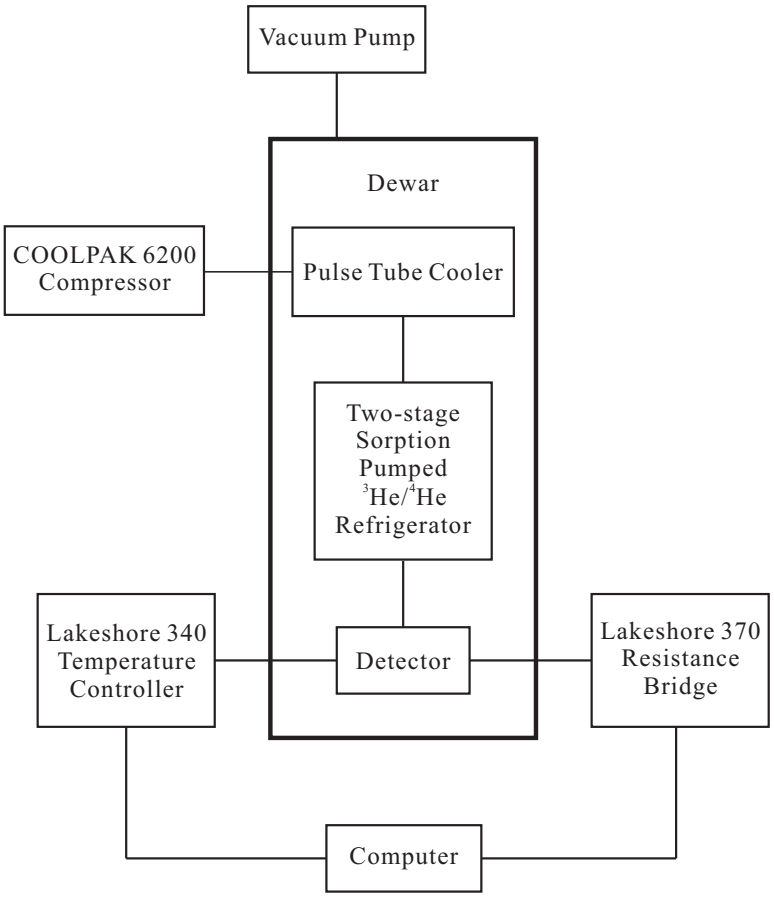

Figure 4.3: Schematic of component interconnections.

4.1 VeriCold He7 Cryostat

4.1.1 Pulse Tube Cooler

Historically, cryogenic systems used liquid cryogens such as liquid helium as the cooling bath. Liquid cryogens have a number of disadvantages, such as the high cost and safety issues in shipping and operation. For applications in space, where cryogens cannot be refilled, life time of the entire system is limited by the hold-time of cryogens. These

problems can be solved by replacing liquid cryogens with a pulse tube cooler (PTC), which cyclically expands gas to cool an object down without consuming liquid cryogens. A two-stage pulse tube cooler can reach liquid helium temperatures (∼4 K), whereas sub-Kelvin temperatures can also be easily achieved by adding a second stage of a refrigerator to a PTC, as in the VeriCold He7 cryostat. Because of its reliability, simplicity, and low cost, pulse tube coolers have become a promising alternative for low temperature applications.

Figure 4.4 shows the schematic of a single-stage pulse tube cooler (from now on referred to as the PTC). Notice that the PTC actually has two stages, each consisting of a regenerator and a pulse tube, but we will introduce the PTC operating principles with the simplest single-stage model. A PTC usually consists of a compressor, a rotary valve, a regenerator, a low-temperature heat exchanger at temperature T_L, a pulse tube, a room-temperature heat exchanger, an orifice, and a buffer volume. The compressor contains helium gas of high pressure, and together with the rotary valve creates pressure oscillations inside the pulse tube by switching between high-pressure, P_H, and low-pressure, P_L. The PTC connects with an external compressor using flexlines. The regenerator contains a porous material of large heat capacity in order to provide good heat exchange with the gas. The pulse tube can be considered to be adiabatic, i.e. no heat exchange happens between the tube and the gas. A complete cooling cycle of the PTC operates as follows:

1. The orifice is closed and the compressor compresses helium gas into the PTC through the high-pressure flexline. When gas passes the regenerator, the gas temperature drops as the regenerator extracts heat from it. With another heat exchange with the low-temperature heat exchanger, the gas temperature drops to T_L.

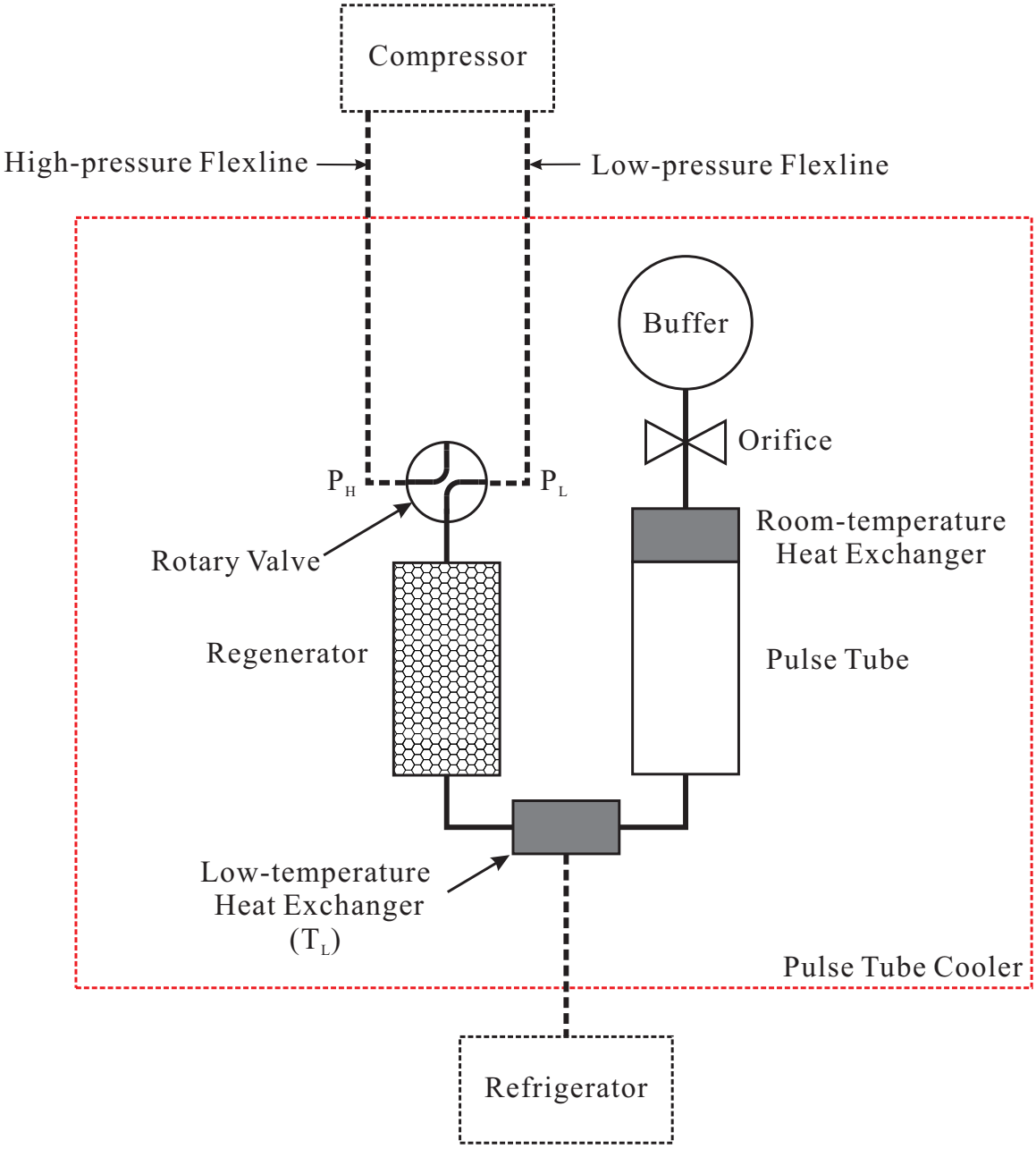

Figure 4.4: Schematic of the pulse tube cooler (inside the red dot line) [59].

2. The gas keeps moving into the pulse tube until pressure in the tube increases to P_H. The increasing pressure cause the gas temperature to rise since the tube is adiabatic. While passing through the room-temperature heat exchanger, the temperature of the gas is further raised.

3. The orifice is now opened, and since the pressure in the buffer volume is just slightly higher than P_H, the gas flows into the buffer volume with negligible change in pressure or temperature.

4. The orifice is closed. The low-pressure pipe of the compressor is switched to the PTC by the rotary valve, decreasing pressure in the pulse tube from P_H to P_L. An adiabatic expansion in the tube causes gas temperature drop to T. Here T is a certain temperature point lower than T_L, as the current pressure P_L is lower than the pressure in step 2 when the gas entered into the tube with the temperature T_L.

5. When expansion stops, the orifice is opened again. The high pressure in the buffer volume pushes gas in the pulse tube towards the compressor. As the gas is still inside the pulse tube, its pressure remains as P_L so that its temperature stays as T.

6. The gas of temperature T enters the low-temperature heat exchanger of temperature T_L and extracts heat from it. This is what creates the cooling power. The gas is heated to T_L.

7. The gas moves through the regenerator where it extracts the heat stored in step 1, and then returns to the compressor waiting for the next cycle.

4.1.2 Two-stage ^{3}He/^{4}He Sorption Pumped Refrigerator

Figure 4.5 shows a schematic of the two-stage ^{3}He/^{4}He sorption pumped refrigerator. Its 4 K plate is connected to the pulse tube cooler. The 300 mK plate is the coldest surface and cools the detector through weak thermal links to the detector mounting block. The ^{4}He pump and ^{3}He pump have been filled with ^{4}He gas and ^{3}He gas respectively, and both contain activate charcoal as absorbant for helium gas. When the pumps are heated to above ∼18 K, the charcoal desorbs helium gas; when the pumps are cooled down below ∼18 K, the charcoal absorbs (pumps on) helium gas. Each pump has a resistor attached which is used to heat it up and a diode monitors its temperature. While heating the pumps is implemented by applying current to the heater resistors, cooling the pumps is achieved by turning on the two heat switches connected to the 4 K plate. The heat switches are gas gap heat switches that enable/disable thermal conduction between two ends by filling/evacuating a gap between them with helium gas, while flow of helium gas is controlled by heating/cooling an active charcoal container absorbed with helium gas. Like the pump, each heat switch has a 10 kΩ resistor attached which is used to heat it up and a diode acts as the thermometer. A 4 V power supply can keep the switch heater at around 20-25 K, which is the "on" state; when power turns off the switch heater will cool down to below ∼10 K after about 15 min, which is the "off" state.

Before starting cooling down, a vacuum pump is used to evacuate the dewar to below 4×10^{-3} mbar. The pulse tube cooler precools the refrigerator from room temperature to ∼4 K, below the critical temperature of ^{4}He of 5.2 K [61]. Then both the pumps are heated to around 100 K to desorb ^{4}He gas and ^{3}He gas from the charcoal [57]. The hot

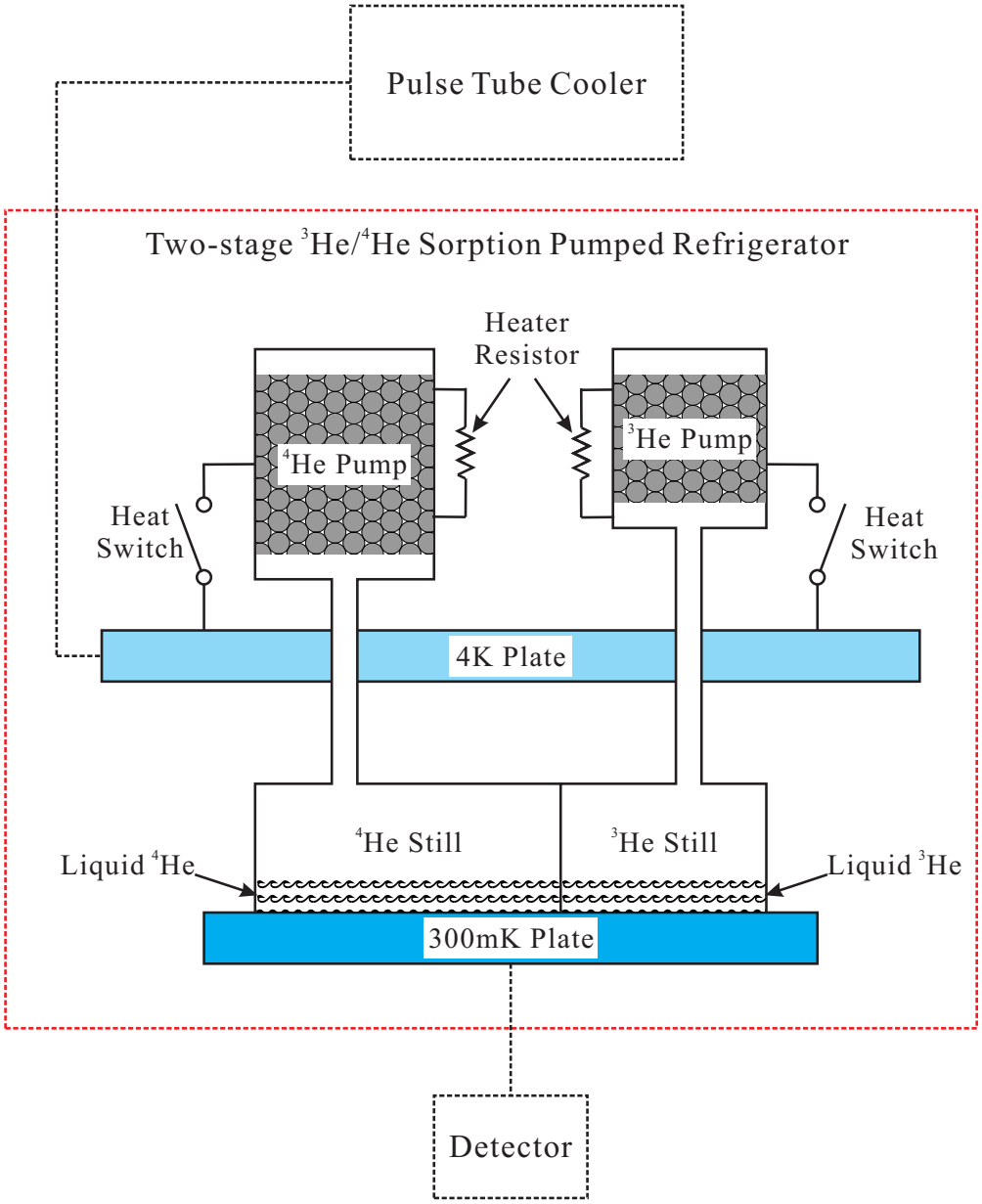

Figure 4.5: Schematic of the two-stage ^{3}He/^{4}He sorption pumped refrigerator [60].

^{4}He gas is cooled down and condenses into liquid in the ^{4}He still. Once all the ^{4}He gas has been liquified, heating of the ^{4}He pump stops and cooling begins by closing the heat switch. As the pump is cooled down below ∼18 K [61], charcoal starts pumping on liquid ^{4}He and the decreasing of pressure of the ^{4}He still leads to decreasing of temperature of liquid ^{4}He. When liquid ^{4}He drops below 3.3 K, the critical temperature of ^{3}He, ^{3}He gas starts to condense into the ^{3}He still. After all liquid ^{4}He in the ^{4}He still has evaporated, heating on the ^{3}He pump stops and the ^{3}He heat switch is closed to cool the ^{3}He pump down. Once the temperature of the ^{3}He pump is below 18 K [61], pumping on liquid ^{3}He starts and pressure in the ^{3}He still drops, consequently the temperature of the 300 mK plate drops further and at the final temperature of 300-350 mK can be achieved and maintained for several days depending on load.

4.2 Accessories

4.2.1 Compressor

A COOLPAK 6200 Compressor [62] was used as the external compressor for the PTC (Figure 4.6). It uses two flexlines, one for high-pressure helium gas and the other for low-pressure helium gas, to connect to the rotary valve on the VeriCold He7 cryostat which provides oscillating pressure to the pulse tube cooler. The compressor has been charged with helium gas at 16 bar and is water cooled by connecting to the the plumbing system of the university. The operation of the compressor is automatically controlled by the computer through a RS 232 serial cable.

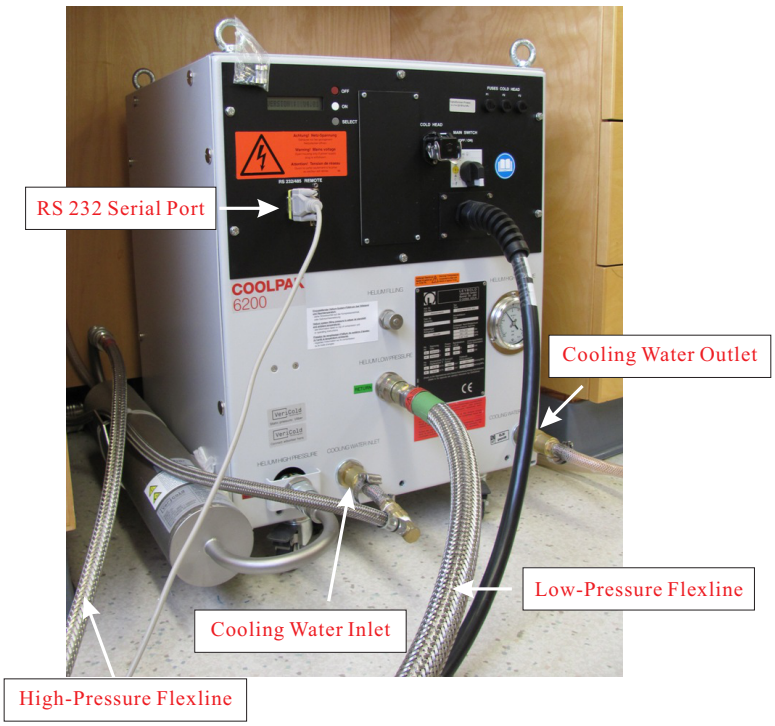

Figure 4.6: The COOLPAK 6200 Compressor.

4.2.2 VeriCold Control Software

Control of the cryostat system is automated by the VeriCold Control software, which reads the temperature sensors and controls the heaters on the refrigerator pumps and heat switches. Figure 4.7 shows a screenshot of the control panel of the software. The "full cool down" function will cool the system to ∼300 mK, while the "cool down" function cools to ∼4 K. Since our TES detectors operate in the range of 4-9 K, we only use the "cool down" function, followed by a series manual operations. To warm up the system, the "stop the pulse tube cooler" button stops the rotary valve and compressor, and the system returns to room temperature after the course of one day.

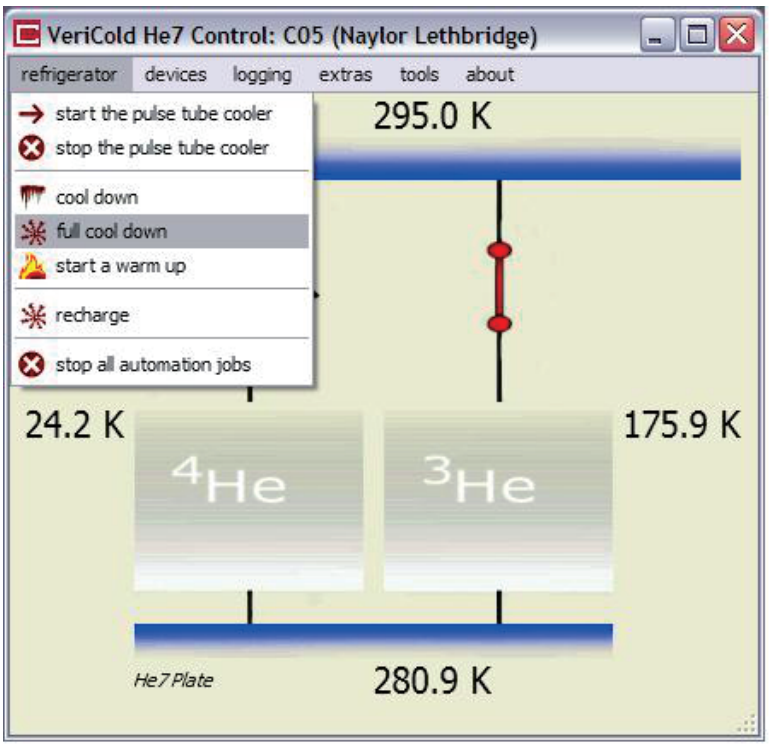

Figure 4.7: Screenshot of the VeriCold Control software.

4.3 System Performance

The system can achieve and remain at temperatures as low as ∼300 mK for about 36 h with a small load, and the refrigerator recycle time is ∼2 h. Cooling down the 300 mK plate to ∼4 K takes about 14 h with a cooling capacity of 330 mW. Figure 4.8 shows the temperature versus time curves of two pumps, two PTC, and three plates in a cooling cycle. From 0 to around 11 hours, the PTC precools the refrigerator from ∼300 K to ∼4 K. From 11 to 19 hours, the two pumps, ^{4}He and ^{3}He, are heated to around 100 K to desorb gas from the charcoal. At around the 19th hour, the ^{4}He pump starts to cool down; later

when its temperature is below ∼18 K, charcoal starts pumping on ^{4}He gas and reduces the temperature of the 300 mK plate. After all the liquid ^{4}He in the ^{4}He still has evaporated, the ^{3}He pump starts cooling down, later the charcoal starts pumping on ^{3}He gas until the final temperature of the 300 mK plate drops to ∼300 mK.

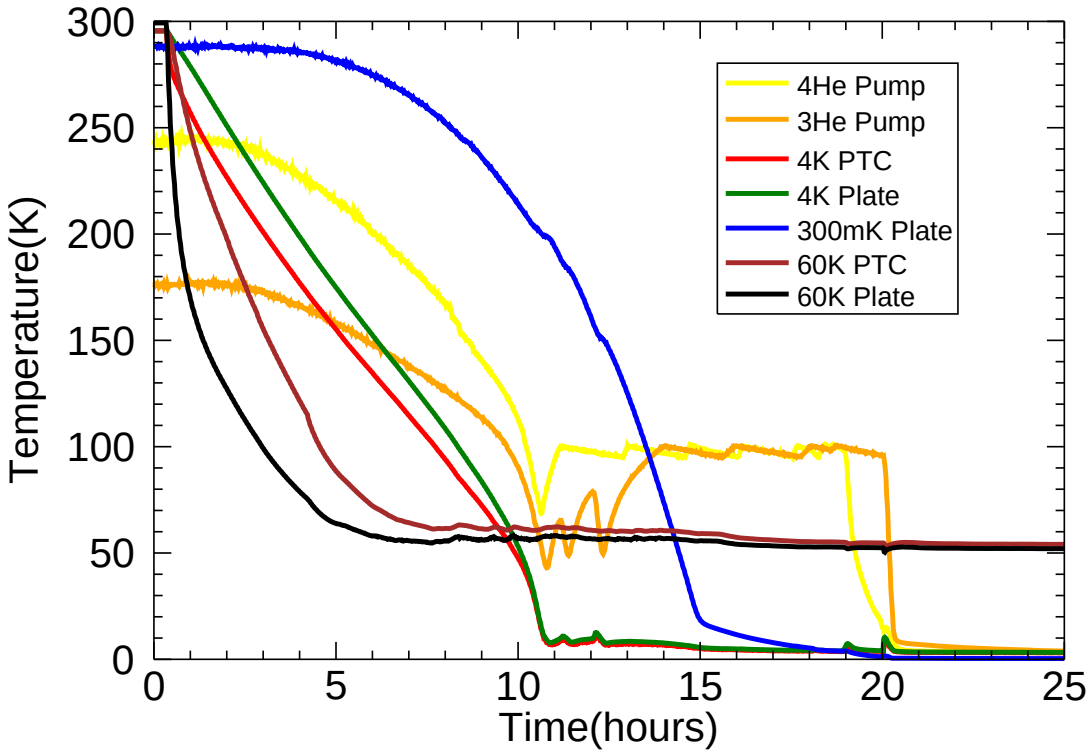

Figure 4.8: An example of the cooling down process.

Chapter 5

Detector Test Facility

This chapter describes in detail the equipments used and the steps involved in evaluating the performance of a detector. The analysis of data obtained from independent detectors and results of their performance are presented in next chapter.

5.1 Detector Installation

After a processed wafer is returned from the Nanofab to our lab in University of Lethbridge, independent detectors are diced from the wafer and glued onto a TO8 header as described in Chapter 3. Al wires are bonded from the Au pads on the detector to the TO8 header (see Figure 3.40). Since it is important to know the transition temperature of the device, a sensitive silicon diode temperature sensor [63] is attached directly to the back of the TO8 header, and connected to the two spare pins of the TO8 header (Figure 5.1). The temperature of the diode is measured using a Lakeshore 340 temperature controller [64] configured in 4-lead mode.

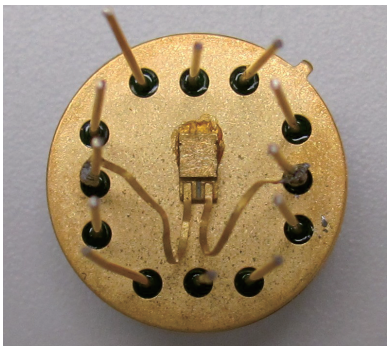

Figure 5.1: A DT-670-SD silicon diode attached on the back of the TO8 header with two leads soldered with TO8 header's pins.

In order to install a detector, the cryostat must first be carefully disassembled. At room temperature and pressure, the three heat shields in the cryostat are removed in sequence as shown in Figure 5.2, allowing access to the cold stage. At this point, the detector used in the previous testing is carefully removed and covered with a protective cap as shown in Figure 5.3. A new detector and its TO8 header are inserted into a square mounting flange (Figure 5.4), the detector is then mated with a detector mounting block which includes a feedhorn (Figure 5.5). The detector block itself is connected with the 300 mK plate through weak thermal links which serves to reduce the thermal noise (Figure 5.6). Since the weak thermal links are fragile it is important not to use excess force in this delicate operation. The final step in the detector assembly is to connect the cryostat wiring harness to the 16-pin connector (Figure 5.6). The harness is automately connected to the external test equipments which are used to evaluate performance of the detector, including the Lakeshore 370 resistance bridge for reading detector resistance and the Lakeshore 340 temperature controller for reading heat sink temperature.

Figure 5.2: Remove and place three heat shields on a clean surface.

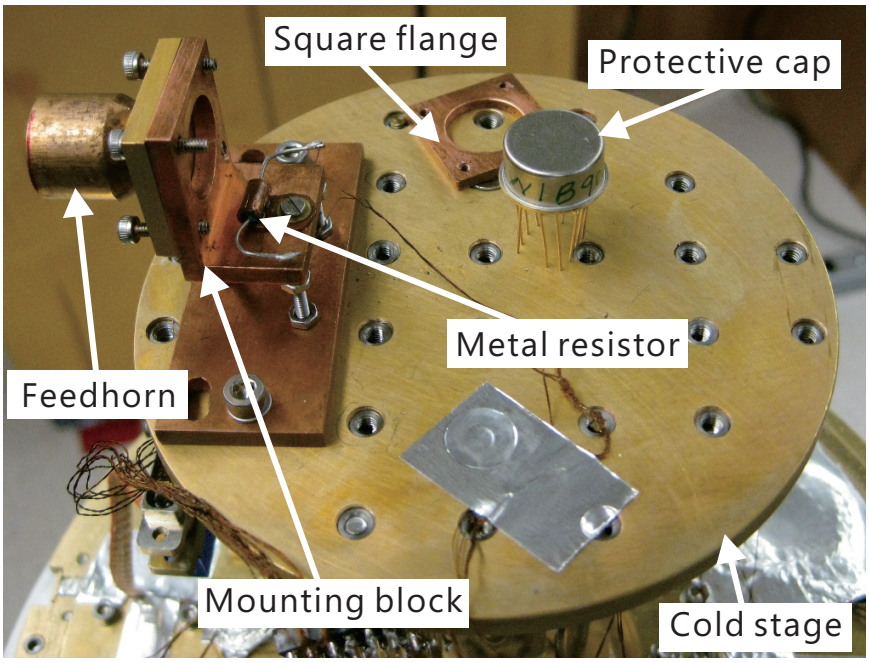

Figure 5.3: Uninstallation of a previous detector, now placed into a protective cap. The metal resistor is used to heat detector to the desired operating temperature.

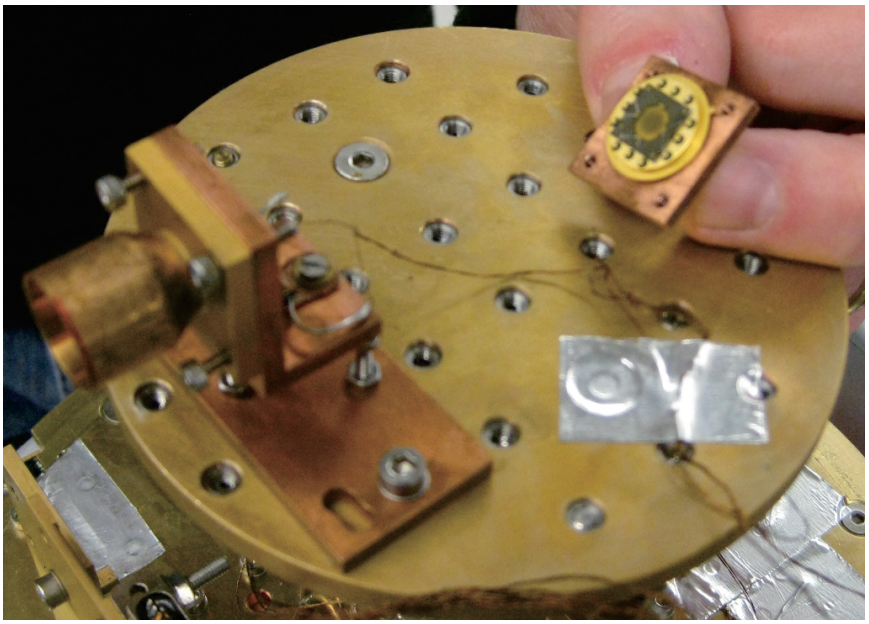

Figure 5.4: A new detector with its TO8 header inserted into a square mounting flange.

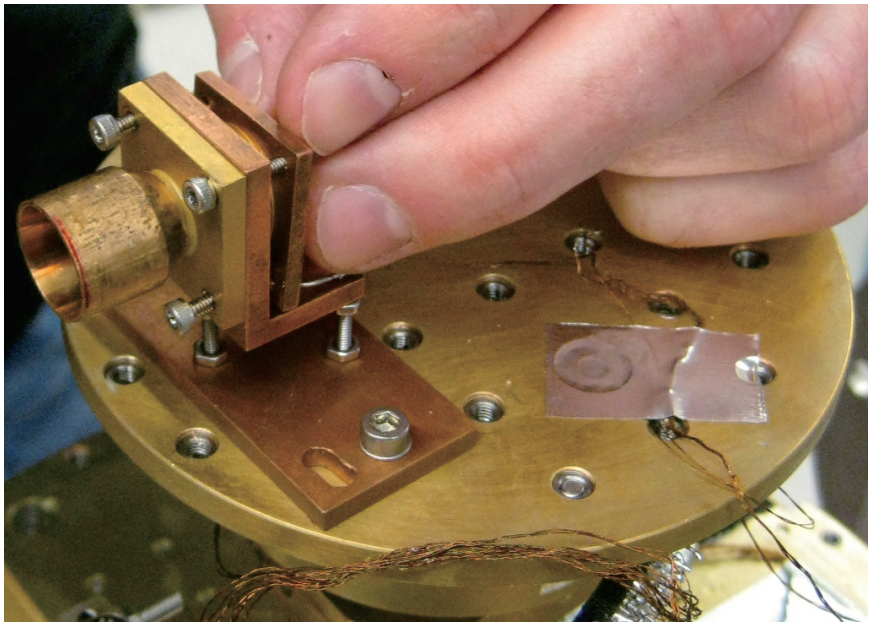

Figure 5.5: Installation of a new detector.

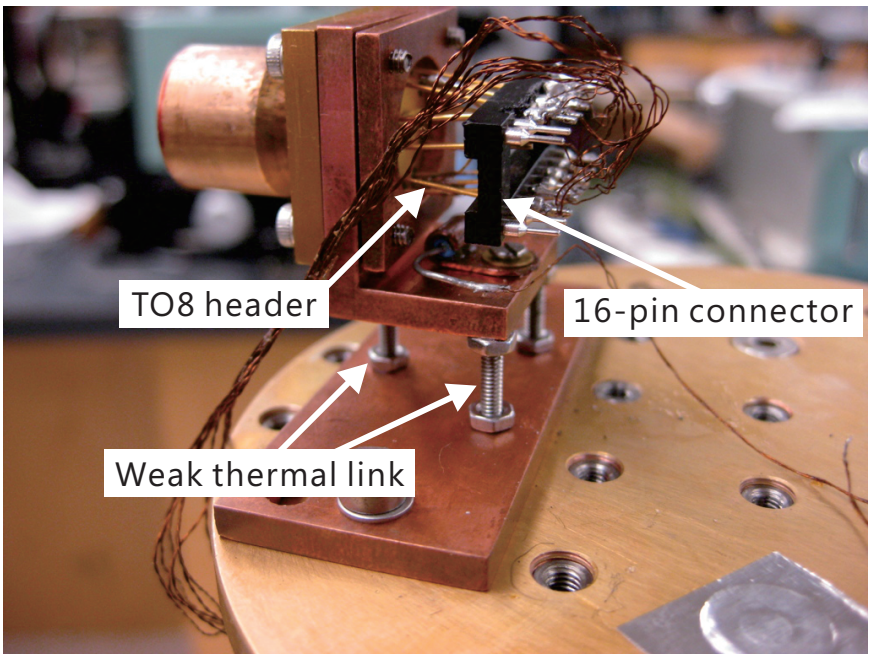

Figure 5.6: A new detector mounted (hidden behind the feedhorn) on the 300 mK plate and the TO8 header plugged onto a 16-pin connector.

In order to test if the detector has been installed correctly, at this stage readings are taken on both Lakeshore 340 and 370 to ensure correct temperature and normal resistance values. Once this has been confirmed, the three heat shields are carefully reassembled without over-tightening any bolts. It is important when install to the inner heat shield that the window does not contact with the feedhorn, which would result in thermal leak and render the detector inoperable. A schematic cross-section of the final assembled cryostat is shown in Figure 5.7. Incident optical power is coupled to the detector through the high density polyethylene (HDPE) window (0.6 mm thick) on the outer heat shield, a 120 cm^{-1} low-pass filter located on the middle heat shield at temperature in the order of 60 K. The cryostat design allows inclusion of two additional filters on the inner heat shield, however, in practice we found that only one 33 cm^{-1} edge filter is required located immediately in

front of the feedhorn.

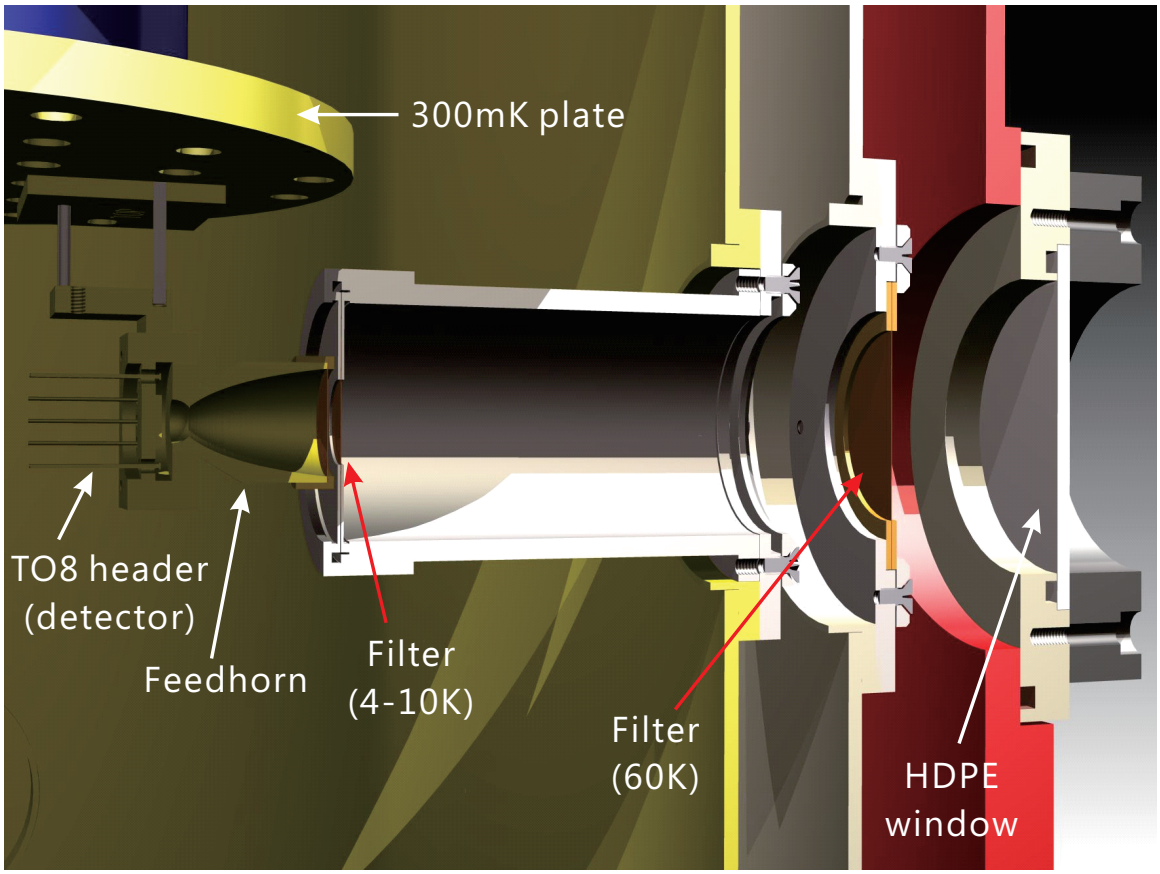

Figure 5.7: CAD visualization demonstrating detector, feedhorn, filters, and window configuration within the cryostat. The detector is mounted on the 300 mK plate with weak thermal links for thermal noise damping. Low-pass edge filters locate at 33 cm^{-1} (4-10 K) and 120 cm^{-1} (60 K).

5.2 Cryostat Operation

After installing a new detector, the cryostat is placed on a stable working deck and the compressor lines are attached to the rotary valve assembly of the pulse tube cooler shown in Figure 5.8. The red line indicates the high-pressure input and the green line is the return line to the compressor.

Figure 5.8: High-pressure and low-pressure flexlines connected to the rotary valve of the pulse tube cooler.

The next step is to evacuate the cryostat using an external vacuum pump shown in lower part of Figure 5.9 which is attached to a vacuum port on top of the cryostat through a flexline, which achieves the inner pressure of 4×10^{-2} mbar. Once the pressure is reached this designed level, the water cooled compressor is turned on and the Vericold control software

activates the cool down of the cryostat; a screenshot of the software is shown in Figure 5.10. Cooling to 4 K takes 12-14 hours, during this time, the control software monitors temperatures of 10 stages and plots temperature versus time curves, which allows to figure out possible problems during cooling down cycle.

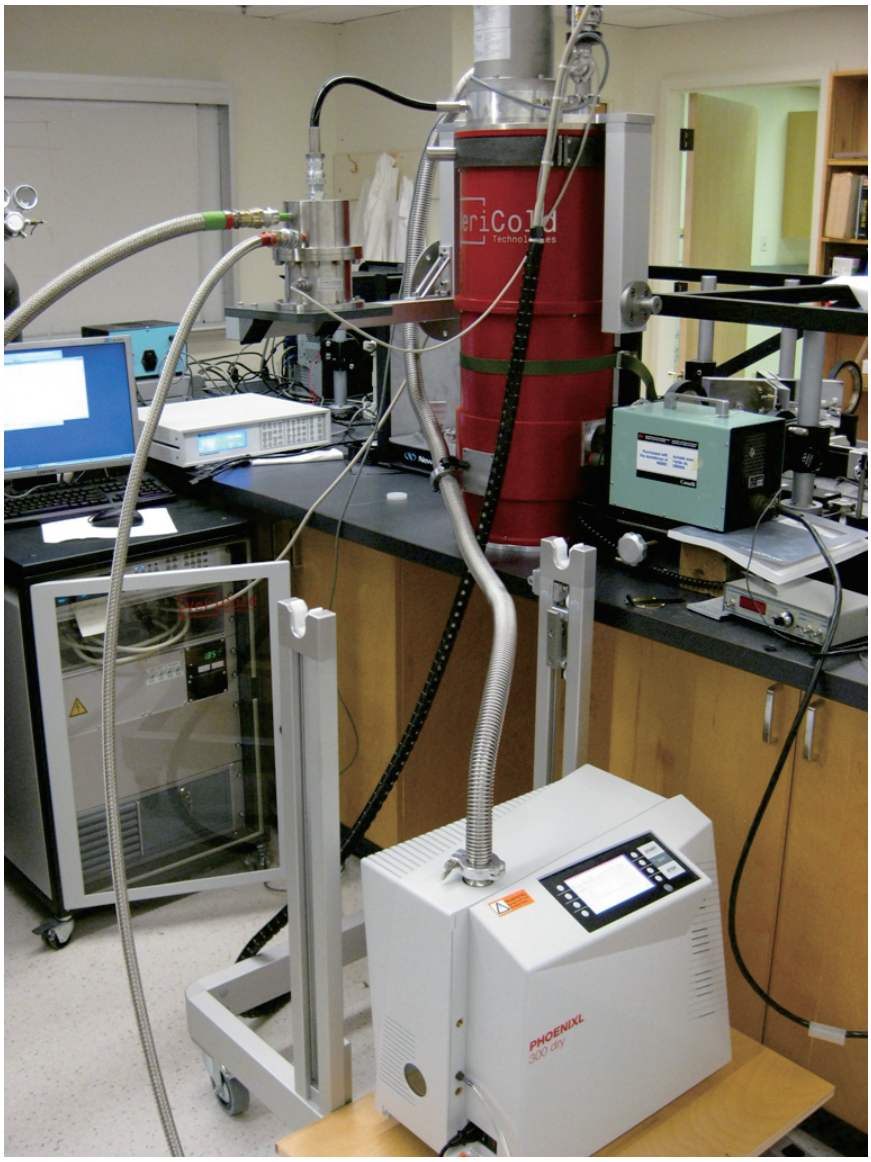

Figure 5.9: A vacuum pump is connected with the cryostat to evacuate its pressure to 4×10^{-2} mbar.

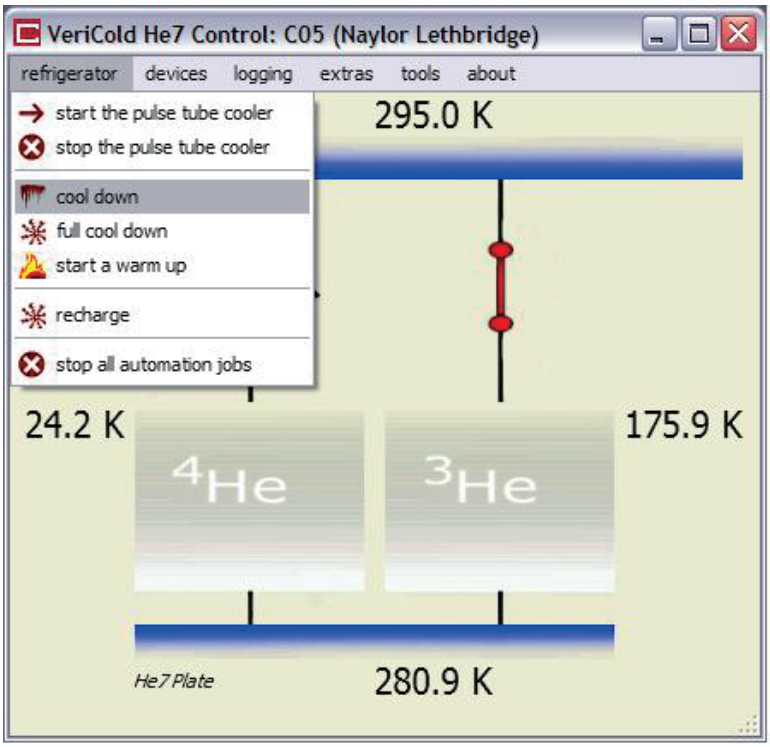

Figure 5.10: Screenshot of the VeriCold Control Software.

5.3 Warm Up Procedure

To warm up the cryostat one simply select "stop the pulse tube cooler" from menu of the VeriCold software (Figure 5.11) and care must be taken to shut down the cryostat system in correct sequence. If this procedure is not observed, then with the compressor still running and the rotary valve not operating, the compressor will vent the helium gas, which will necessitate a recharge of helium. It normally takes about ∼24 h to warm up, but this process can be expedited by back-filling the vacuum chamber with helium gas. The final step is to bring the internal pressure of the cryostat to atmosphere pressure. A small hole

in a cap located on one of the vacuum ports of the cryostat allows air to slowing enter the cryostat. When the hissing of flowing air disappears, the cryostat is at atmosphere pressure, and a new detector can be installed by repeating all steps in Section 5.2.

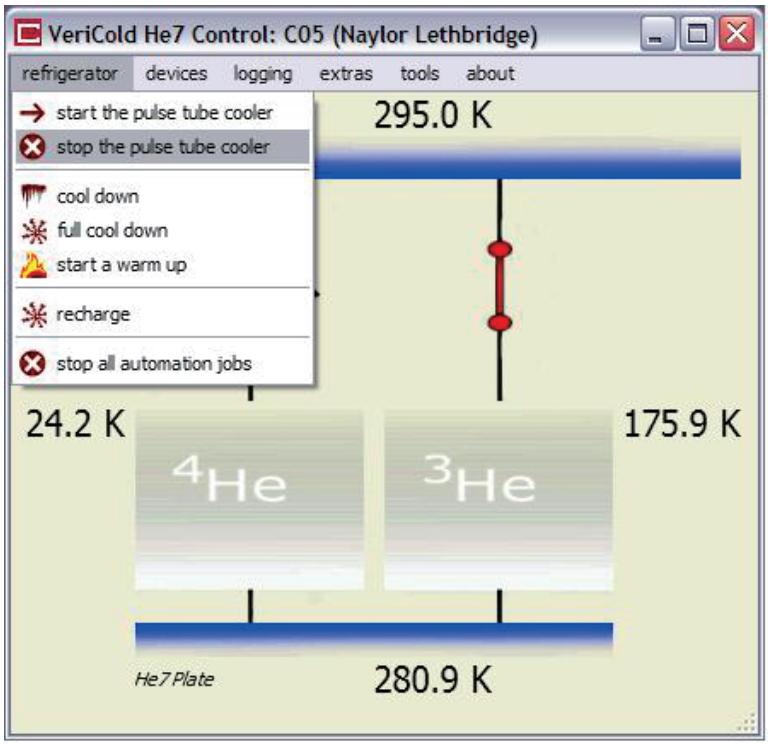

Figure 5.11: Stop the pulse tube cooler with software.

Chapter 6

TES Performance

6.1 Introduction

This chapter describes the three separate tests that I have conducted to evaluate the performance of the TES detectors that I developed in Nanofab, namely, measuring the temperature dependence of the superconducting transition and determining the noise performance and frequency response of these detectors. For each test the design of the experiment and the data acquisition process, analysis and results are presented. Section 6.2 presents the analysis of the R-T characteristics of a device, which determines its ultimate sensitivity, and includes the discussion of what determines the transition temperature, T_c. Section 6.3 describes the measurement of the detector responsivity and noise equivalent power (NEP). Section 6.4 describes the measurement of the time constant as a result of the frequency response.

6.2 R-T Characteristics

In order to determine the variation of resistance with temperature through the sharp superconducting transition, it is essential to control accurately the temperature of the device while measuring its resistance. Furthermore, the act of measuring the resistance of the device must not significantly heat the device.

The experimental configuration is schematically shown in Figure 6.1. A Lakeshore 340 cryogenic temperature controller is used to vary the temperature of the detector by heating the metal resistor mounted to the detector assembly as shown in Figure 6.3. The detector is suspended from the cryostat cold plate by a weak thermal link seen in Figure 6.3, which provides cooling when current is applied to the metal resistor. By this method the temperature of the detector can be varied between 4 and 10 K, which covers the range of the possible transition temperatures for Nb. The Lakeshore 340 also measures the temperature of the detector by means of the diode thermometer on the back of the TO8 header. A sensitive low current four wire Lakshore 370 resistance bridge measures the resistances of the four individual sensors on the TES device.

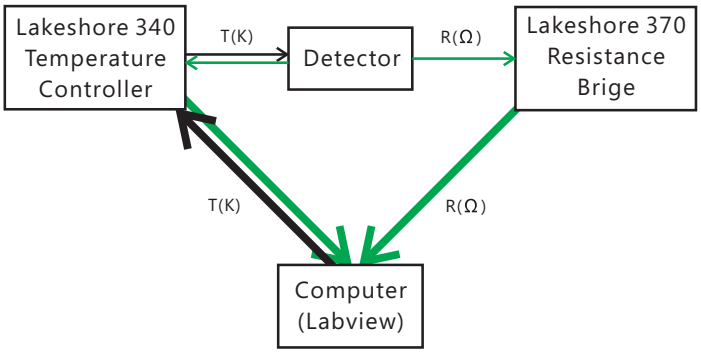

Figure 6.1: Experimental configuration for R-T characteristic measurements with flow of control (black) and data (green).

All of the control and data acquisition software are written in LabVIEW [65] and fully automated so that an efficient and extensive detector test can be conducted using the LabVIEW programs.

6.2.1 Transition Temperature and Sensitivity

R-T measurements were obtained from a total of 15 detectors consisting of 59 sensors over a wide range of transition temperatures from 3.5 K to 8.5 K. An example of a measured R-T characteristic obtained using a bow-tie-shaped sensor (see Figure 3.21) is displayed in Figure 6.2. This bow-tie-shaped sensor of thickness 20 nm shows the maximum transition slope of ∼49 kΩ/K (Figure 6.3), or a logarithmic sensitivity α = dlogR/dlogT of ∼500, at T_c of 7.25 K with an operating resistance of ∼1.9 kΩ.

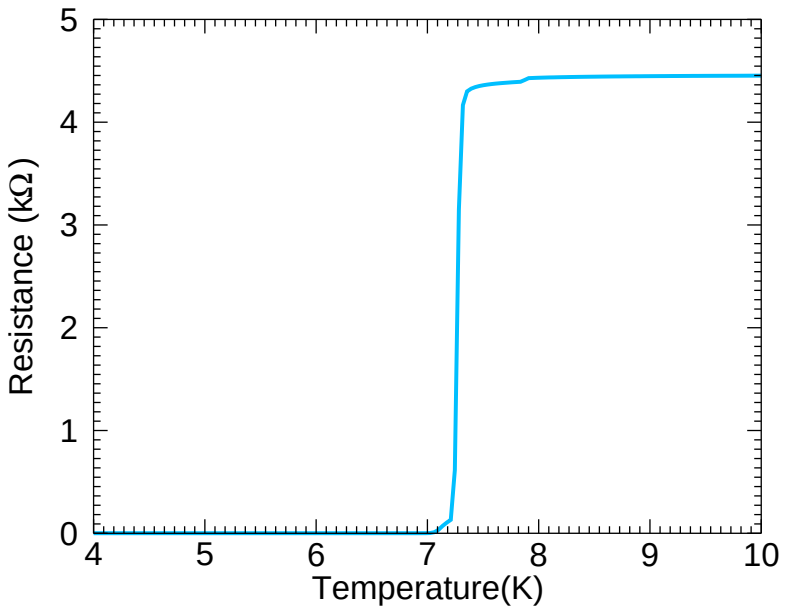

Figure 6.2: R-T curve of a 20 nm thick Nb device.

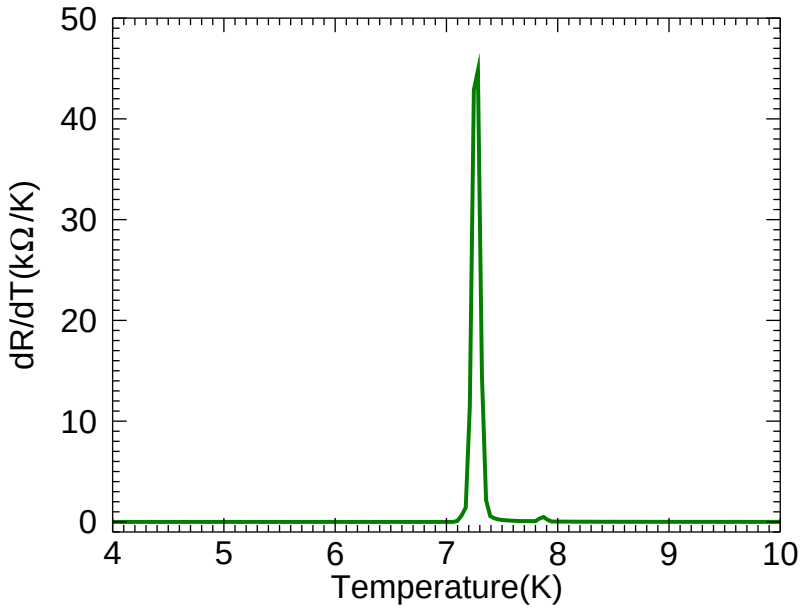

Figure 6.3: Linear sensitivity of a 20 nm thick Nb device.

6.2.2 Film Thickness and Sputtering Pressure Effects on T_c

Our results confirm the observations by other researches [16] that two factors can significantly affect transition temperature T_c of thin Nb films. The first is the thickness of the Nb film: for films thinner than 100 nm T_c drops with decreasing film thickness, and further more, this T_c reduction is more significant for film thickness below 50 nm [16]. The second factor, mentioned in Chapter 3, is that the properties of the sputtered thin film show a very strong dependence on the sputtering pressure of the argon buffer gas used in the deposition process [66].

To study the variation of film thickness and sputtering pressure on T_c, we measured and compared the transition temperatures of 8 devices with Nb thickness ranging from 20

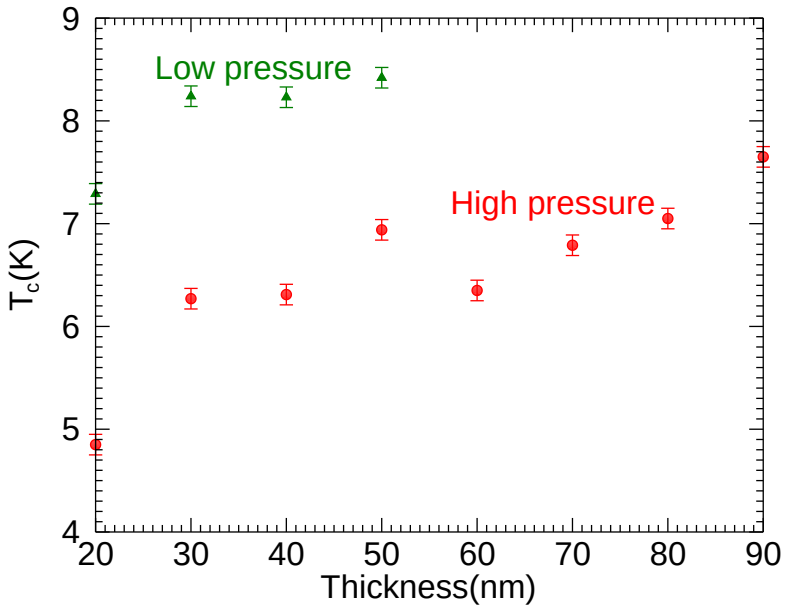

Figure 6.4: Transition temperature T_c of Nb films as a function of thickness and sputtering pressure.

nm to 90 nm. These devices were manufactured under two different sputtering pressure regimes, 7 mTorr and 0.8 mTorr. The results are shown in Figure 6.4.

The dependence of transition temperature on film thickness and sputtering pressure is clearly evident in Figure 6.4. An explanation of the higher transition temperature obtained from lower sputtering pressure can be contributed to the achievement of better crystal structure of films under lower pressure [66]. The dependence of T_c on film thickness has been reported by others [66], [16], is thought to be due to the proximity effect between the central superconducting layer and the non-superconducting layers on the top and the bottom surfaces of the films [16]. However, these important results confirm the early work and provide a recipe for future detector design parameters, so that a superconducting

transition temperature can be tuned for a specific application by carefully controlling the parameters during the deposition process.

As shown in Chapter 2, a lower T_c is preferred since it reduces both the thermal fluctuation and the Johnson noise (see Equation 2.16 and 2.17). From Figure 6. it seems prefer a higher sputtering pressure. However, the electrical resistivity of the Nb film of given thickness seems to increase with sputtering pressure, and thus favoring a lower sputtering pressure. These results indicate there exists a complex tradeoff between sputtering pressure, film thickness, T_c, and device resistance. Ultimately, the geometry of the device determines the resistance, however, since a single wafer run is fabricated at a fixed sputtering pressure and film thickness, time did not permit us to explore this complex tradeoff of space. Since lower resistivity leads to more sensitive detectors, a low sputtering pressure is to be preferred.

6.2.3 Impact of Gold Lead on Temperature Transition

To achieve a sharp transition it is important that all the devices are in the transition which is equivalent to requiring that there should be no temperature gradient across the Nb film. One method to ensure a sharp transition is to overcoat the non-detecting part of the device with Au, which increases the thermal conductivity to the device itself, ensuring that only the Nb component is remaining at transition. To study this effect, we fabricated a few devices which consist of two Nb sensors partially covered with thin Au leads, and the other two without such leads as shown in Figure 6.5. The measured R-T curves for the four sensors are shown in Figure 6.6. It can be seen that as the optical load increases, the transition sharpness of the pure Nb sensors decreases, while the Au covered sensors remain

the same. This is to be expected as the Au covered sensors can more effectively conduct the additional power to the heat sink and remain relatively stable even at higher optical load.

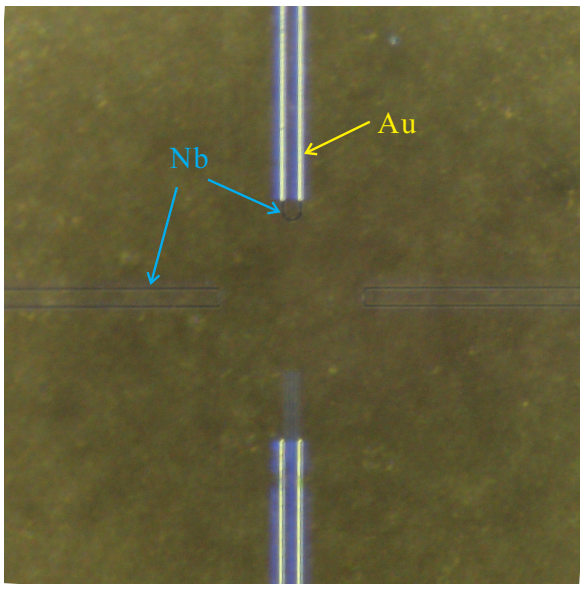

Figure 6.5: Microscope graph of Nb sensors partially covered with Au leads and without Au leads.

The impact of the Au leads on the response to changing optical power is shown in Figure 6.6. The optical power were varied by viewing a black body and a relatively high power microwave source positioned at two distances from the detector system. In all cases the pure Nb sensor exhibited a single transition which broadens out under increasing power. At the same time it can be seen that the Au coated sensor exhibited two transitions, but the transition remains steep independent of optical load. The higher transition is due to the Nb itself, while the lower transition is due to the proximity effect between the Au and the Nb layers [67].

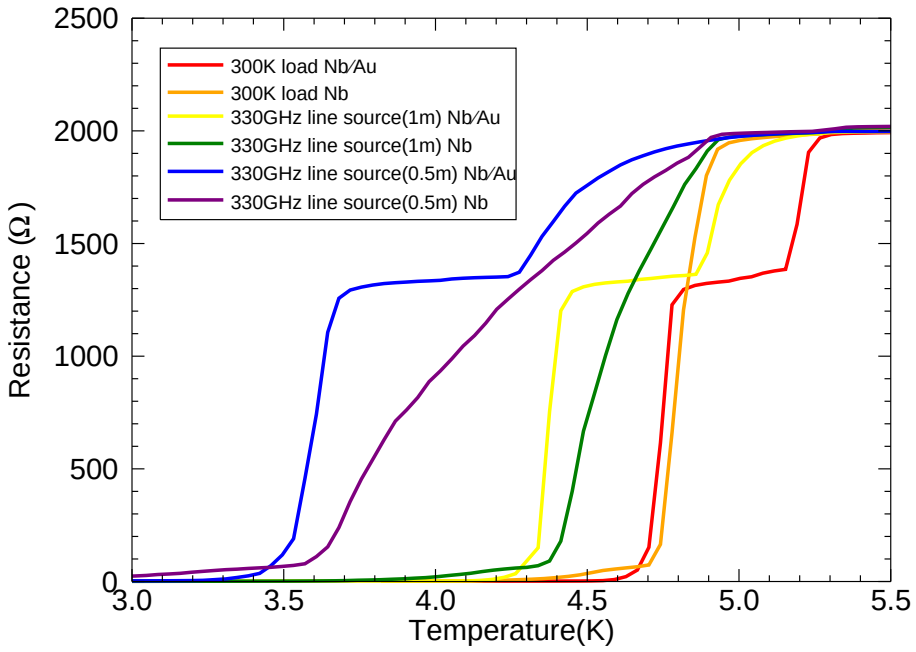

Figure 6.6: R-T curves of two 20 nm sensors (one with pure Nb and the other covered with Au) viewing different optical loads. The pure Nb sensor exhibits a single transition which broadens out under increasing power. The Au covered sensor retains a sharp transition independent of optical load but two transitions.

6.3 Noise Performance

The noise performance of the detectors was evaluated using a standard procedure as shown in Figure 6.7. Incident power from a blackbody source [68] at temperature of 923 K, is modulated by an ambient 6-blade chopper [69]. The chopping frequency is computer controlled through a NI USB-6221 DAQ (data acquisition) device [70] and can be varied from 0 to 100 Hz. As mentioned previously, because of the higher resistance, the signal from the TES detectors can be read out by a simple operational amplifier circuit, which is

presented in Appendix A. Both the modulated signal and noise voltages are measured by a SR760 spectrum analyzer [71] after passing through a SR560 low-noise voltage preamplifier [72]. The schematic of the control and data acquisition components is shown in Figure 6.7. All components are controlled through LabVIEW programs that are given in Appendix B.

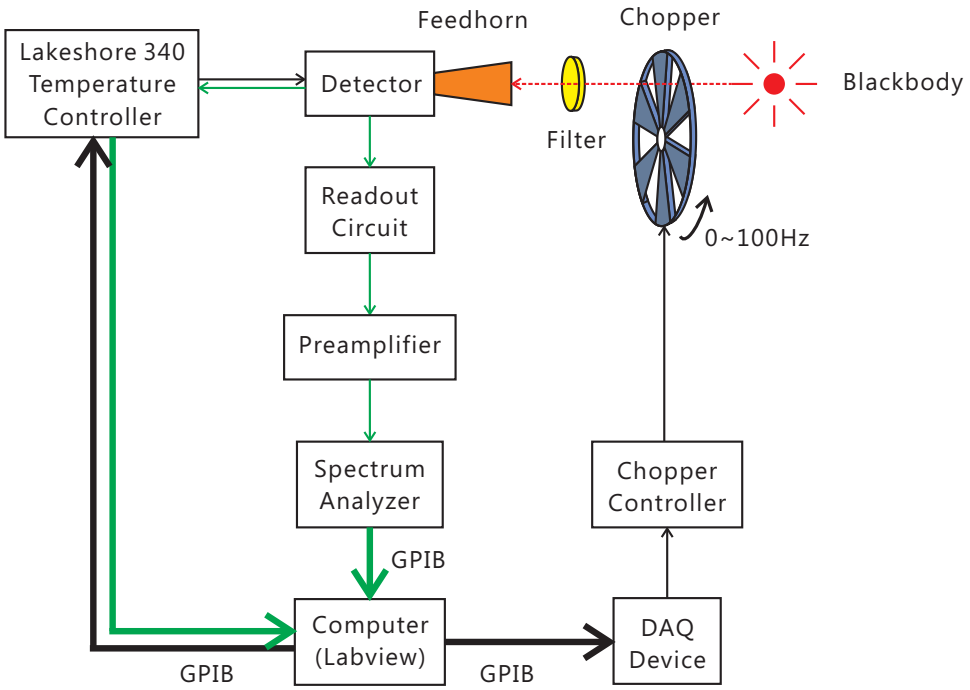

Figure 6.7: Experimental configuration for noise performance measurements.

6.3.1 Incident Signal Power

The NEP is calculated using Equation 1.8, which requires the acknowledge of rms signal power P_{rms} and the noise bandwidth Δf. The rms signal power incident on detector can be written as [2]:

$$P_{rms} = \frac{A_s A_d}{r^2} \tau_w \tau_{f1} \tau_{f2} F_F \int_{\nu_1}^{\nu_2} L(\nu, T_B) - L(\nu, T_C)\, d\nu \quad [W]. \tag{6.1}$$

Here $A_s = \pi(5\text{ mm})^2$ is the area of the blackbody source aperture, $A_d = \pi(5\text{ mm})^2$ is the area of the feedhorn; τ_w (= 0.9), τ_{f1} (= 0.7), and τ_{f2} (= 0.7) are the transmissions, of the thin HDPE window and the two low-pass edge filters on the cryostat, respectively; r is the distance of the cryostat window from the blackbody source aperture (0.2 m); F_F is the form factor that is used to convert a peak-to-peak square wave signal to an rms signal (0.45); ν_1 is the high-pass cutoff frequency determined by the exit aperture of the feedhorn (0.667 cm^{-1} or 20GHz); ν_2 is the low-pass cutoff frequency determined by the 33 cm^{-1} long-pass filter (1THz); T_B (= 923 K) and T_C (= 296 K) are the temperature of the the blackbody source and the chopper blades, respectively; $L(\nu,\, T_B)$ and $L(\nu,\, T_C)$ are the spectral radiance of the blackbody source and the chopper blades respectively, given by [8]:

$$L(\nu, T) = \frac{2h\nu^3}{c^2(e^{h\nu/kT} - 1)} \quad [Wm^{-2}Hz^{-1}ster^{-1}], \tag{6.2}$$

where $h = 6.626 \times 10^{34}$ $[J \cdot s]$ is Planck's constant, ν is the frequency of the incident power, $c = 2.998 \times 10^8$ $[m \cdot s^{-1}]$ is the speed of light, $k = 1.38 \times 10^{-23}$ $[J \cdot K^{-1}]$ is Boltzmann's constant, and T is temperature.

Substituting Equation 6.2 and all the values discussed above into Equation 6.1, results a modulated rms power, P_{rms}, of 1.96 nW.

6.3.2 Noise Measurement

In order to calculate the signal-to-noise ratio (SNR) which is required to determine the NEP of the detector, we need to measure the signal and noise separately. For practical

reason we chose to measure the noise first. To measure the noise, a piece of ECCOSORB® absorbing material [73] is placed in front of the cryostat window to ensure the background noise is only contributed by sources within the cryostat. The LabVIEW program sets the spectrum analyzer to scan from 0 to 97.5 Hz and record the rms power spectral density (PSD) ($V/\sqrt{Hz}$) at each frequency point by averaging 20 samples. After integrating for 4 s, the PSD of 400 frequency points are stored as a noise array for computing the final SNR.

6.3.3 Signal Measurement

The signal measurement is obtained by removing the ECCOSORB® absorber and measuring the modulated power that is seen by the detector when viewing, alternately, the hot blackbody source and the ambient chopper blade. As described earlier, the chopping frequency is controlled by the output voltage of the NI USB-6221 DAQ device. The system is set to provide a full-scale control voltage of 5 VDC for the 0-400 Hz possible with the SR540 model frequency range. Thus, each 1 Hz increment corresponds to 0.0125 volts. In the LabVIEW program (Appendix B) the desired chopping frequency, f_{chop}, is achieved by setting the chopper control voltage $V_{control}$ to:

$$V_{control} = 0.0125 f_{chop} = 0.0125(f_{min} + n \cdot step), \tag{6.3}$$

where f_{min} is the starting or minimum chopping frequency, n is the current iteration number, and step is the frequency increments.

For the NEP measurements, the chopping frequency is set to start at 1 Hz and finish at 97 Hz in 4 Hz increments. At each chopping frequency, the spectrum analyzer computes the rms signal spectrum (V_{rms}) by averaging 10 samples, on the same 1-97.5

Hz frequency scale as the noise measurement. The rms signal spectrum is divided by the previously taken noise array to obtain the SNR array. The maximum SNR and its associated modulating frequency is recorded. The minimum NEP is then computed using Equation 1.8. The chopped signal measured at this time is also used to calculate the responsivity in the following section. By adjusting the temperature of the detector in steps of 200 mK, around the transition temperature, it is possible to optimize the NEP, and to date, the lowest NEP has been obtained is of 0.83 pW/Hz$^{1/2}$ from an 80 nm meander shape device at 7.12 K.

6.4 Responsivity

The voltage responsivity for each detector is calculated using Equation 1.4, where the modulated signal power of 1.96 nW is used. The corresponding voltage from the detector is determined from the measurement of the output signal from the detector electronics after taking into account the gain of the preamplifier circuit, G_1, and the external gain G_2 from the SR560 low-noise voltage preamplifier as:

$$V_{detector} = \frac{V_{measured}}{G_1 G_2}. \tag{6.4}$$

Since $G_1 = 10^5/R_{TES}$ (see Appendix A) is inversely proportional to the resistance of the TES, which cannot be measured at the time the chopped signal is being measured, this introduces an uncertainty into the final determination of the detector voltage, and thus the responsivity. Although there is some uncertainty in the derived responsivity, typical voltage responsivity values of a few kV/W, and corresponding current responsivity of a few

A/W are observed. The highest voltage responsivity we have obtained was from a 30 nm bow-tie shape device at 8.18 K which yields a voltage responsivity of 15.24 kV/W or in terms of a current responsivity of 12.7 A/W.

6.5 Discussion

There are many factors will impact the NEP, for example, the geometry of the device, Nb film thickness, inclusion of Au leads, the variation in sputtering pressure; the parameter space is indeed large. Since the device fabrication process is intensive and involves many steps, there was insufficient time to fill out all the parameter space. Table 6.1 lists the NEPs measured for devices of a fixed bow-tie geometry, in which the variation of film thickness, sputtering pressure, and Au overcoating were changed. There are no obvious distinctions on figures of merit of different devices except for the 30 nm device, which shows a comparably higher responsivity, however, I believe it is a unique result rather than a routine. While further work is needed to explore these dependencies, one can see that NEPs of a few pW/$\sqrt{Hz}$ are routinely being measured with different fabrication parameters.

Table 6.1: Measured parameters of bow-tie shaped devices with different Nb thickness, operating temperature, and sputtering pressure.

Thickness (nm)	Temperature (K)	Best NEP (W/Hz$^{1/2}$)	Responsivity (kV/W)	Time Constant (ms)	Sputtering pressure	Covered with Au
20	7.22	2.36	1.63	0.71	Low	N
30	8.22	1.42	10.94	0.63	Low	Y
40	8.20	1.75	3.78	0.63	Low	N
50	8.43	1.75	2.19	0.92	Low	Y
50	6.87	2.16	1.72	0.49	High	Y
80	7.06	1.60	2.72	0.62	High	N
90	7.53	2.01	1.13	0.92	High	Y

6.6 Frequency Response

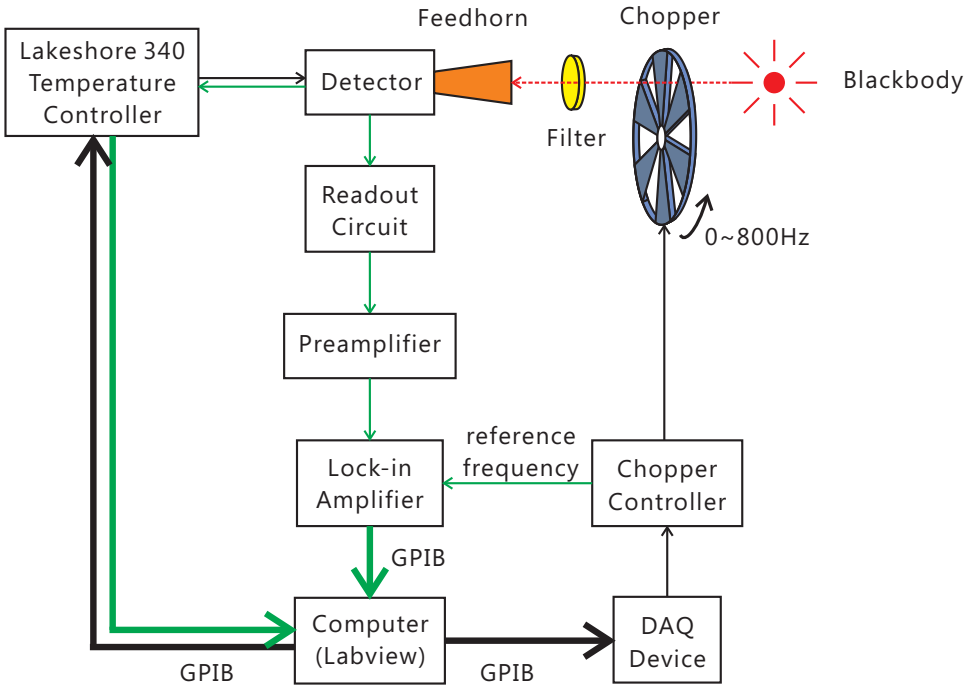

Figure 6.8: Experimental configuration for frequency response measurements.

The frequency response is determined using essentially the same experimental configuration as for the noise performance measurements except the spectrum analyzer is replaced by an SR830 lock-in amplifier [74] (Figure 6.8). The chopping frequency can be varied between 0 and 800 Hz, and the reference frequency signal from the chopper controller is used as an input to the lock-in amplifier. Figure 6.9 shows an example of the normalized frequency response for an 80 nm square-loop device (see Figure 3.21). The cutoff frequency, f_{co}, defined at the -3 dB point, is 259 Hz and the corresponding time constant τ is 0.62 ms.

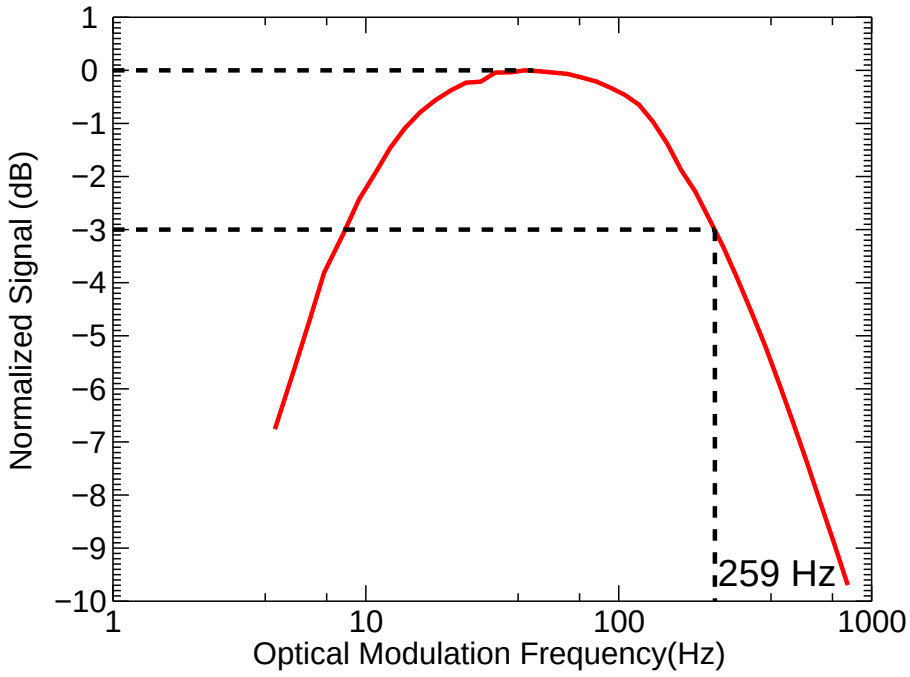

Figure 6.9: Normalized frequency response for an 80 nm square-loop device viewing a blackbody source.

The measured time constants for all the single-pixel devices fall in the range of 0.43 - 0.92 ms. Table 6.1 provides no correlation between frequency response and sensor parameters such as thickness, Au leads, or sputtering pressure. These results indicate that the contribution to the total heat capacity of the device from the metalized components is negligible, and that the heat capacity is dominated by the contribution from the Si_3N_4 membrane. This conclusion is supported by the result obtained from studying the performance of the central pixel of a 3×3 multi-pixel device. A time constant of 0.33 ms has been observed, which is due to the reduced heat capacity from the smaller Si_3N_4 membrane. Thus, it is clear that by fabricating devices on thinner or mesh-structured Si_3N_4 membranes

we should be able to make faster devices.

6.7 Summary

This chapter has presented the results from evaluating the performance from a number of TES devices. The key detector parameters of NEP, responsivity, and frequency response have been discussed. These results show that the TES devices we have built have achieved the design goals of low noise, high sensitivity, fast response, and importantly, their compatibility with cryogen-free systems.

Chapter 7

Conclusions and Future Work

The thesis reports on the work I have done to develop a detector fabrication capacity for Astronomical Instrumentation Group in the University of Lethbridge. We are the first group from University of Lethbridge to use the Nanofab facility to fabricate devices. During the period of pursuing my Master's degree, I have learned to use an extensive range of equipment in the microfabrication process including: design of photomasks, deposition of thin films, lift-off techniques, wet etching, and plasma etching, etc. There are a large number of variables in this process, and we have chosen to focus subsets which are considered to be important including: the geometries of TES, the Nb film thickness, the sputtering pressure, and Au overcoating. We have fabricated a number of devices and evaluated their performance in our laboratory in University of Lethbridge. The results show that we are able to fabricate devices with NEPs of a few pW/$\sqrt{Hz}$ from a successful flow process. The final device yield at the Nanofab facility exceed more than 90%. Some devices are lost in the dicing, mounting, wire-bonding, integration, and assembly of the final detector in our

laboratory at University of Lethbridge. We expect that our success rate will increase as we move to thinner 300 μm wafer fabrication which simplifies the dicing process.

Not only have our detectors achieved excellent NEP, but also because of the reduced heat capacity from the Si_3N_4 membrane, our devices have a superior frequency response being at least an order of magnitude faster than the standard bolometer. Further more, we expect that faster devices can be fabricated. A key result of this work is that we have been able to show our devices can be operated in a cryogenic-free system. This not only removes the reliance on expensive liquid cryogens, but also improves the efficiency of operating such devices in our laboratory setting. To our knowledge, we are the first group to operate the TES device directly with a PTC cryogen-free system.

My thesis has laid the ground for a new area of research within the Astronomical Instrumentation Group. Until now our group purchased detectors from manufacturers, but they lag behind state-of-the-art devices. This research all began when my supervisor, Professor David Naylor, was invited to give a lecture to the Department of Physics and Astronomy at the University of Alberta. During this trip, he visited the Nanofab and was extremely impressed not only by the infrastructure but also by the staff. On returning from this inspiring trip, he discussed with me about possibility of making some new detectors, which ultimately became my thesis' topic.

I have shown that the sensitivity of detectors depends upon several factors. While I have explored a small part of the available parameter space, much work remains to be done. The next logical step is to move to fabricate devices on thinner wafers, which will lead to higher packing density of pixels, faster time response. We have considered the possibility

of moving to a spiderweb membrane or other geometries. None of this work would have been possible without the access to, and abilities of the Nanofab of University of Alberta. Although this is a new field for our group, we have successfully produced devices that are competitive with the best that are commercially available using old technologies.

The future work will tune the key parameters related to detector performance, such as adjusting Nb film thickness for a sufficiently low transition temperature, choosing a low sputtering pressure to improve sensitivity, and making spiderweb devices to reduce response time constant. We will also focus on improving the proficiency of the testing process, such as the speeding-up of cryostat cooling down cycle, replacing the current used Lakeshore resistance bridge for a single detector test with a more efficient system that can test four detectors at one time. The next generation devices will find extensive use in supporting the research activities of the AIG group.

Appendix A

TES Preamplifier Circuit

SQUID (Superconducting Quantum Interference Device) is widely used to provide bias voltage and amplify the output current for low-resistance TES, but for our high-resistance TES aiming at applications of considerably high performance the cost of using SQUID makes it impractical. We chose a simple homemade operational amplifier (op-amp) circuit [54] as an alternative to SQUID and its performance was sufficient for our current prototype TES devices. We have also planned to replace the op-amp circuit with a transformer-coupled circuit for better noise performance in future.

The room-temperature op-amp circuit was fabricated on a printed circuit board (PCB) mounted inside of an Al shielding box (Figure A.1). The box is placed at room-temperature outside the cryostat where detector works. The circuit has four identical channels and each of them reads the output voltage of one sensor from a single-pixel device containing four different shaped sensors. Figure A.2 shows the schematic of the preamplifier circuit for one channel. The top and bottom parts are two voltage-regulator circuits, built

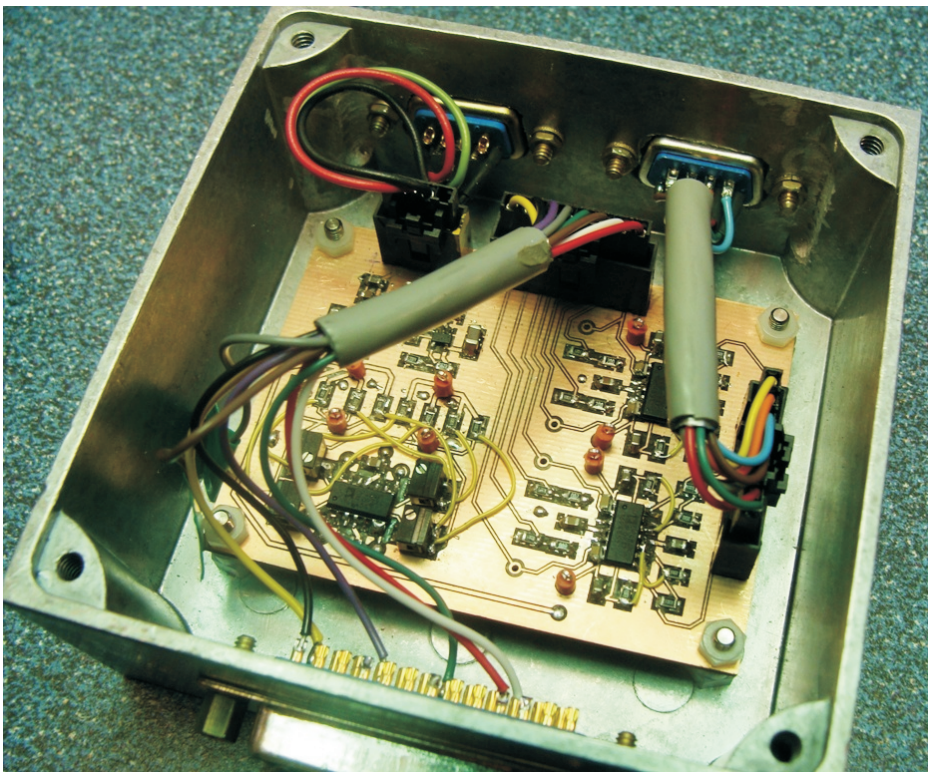

Figure A.1: Op-amp circuit inside of an Al shielding box.

by a LT1761 [75] and a LT1964 regulator [76] respectively. They regulate the +12V/-12V voltage from a DC-power supply [77] to the constant value of +11V/-11V as voltage power supply to the circuit. The middle part is a two-stage preamplifier circuit made by three op-amps of a quad OP484 chip [78]. The left op-amp functions as a voltage follower to the adjusted input voltage of 0.52V from the pot resistor, the middle one is the first-stage inverting amplifier, and the right is the second-stage non-inverting amplifier. The constant bias voltage V_{bias} of 10 mv is obtained in between the voltage follower and the first-stage amplifier by paralleling a shunt resistor (R_9 = 20 Ω) with the TES (operating resistance of 102 or 103 Ω).

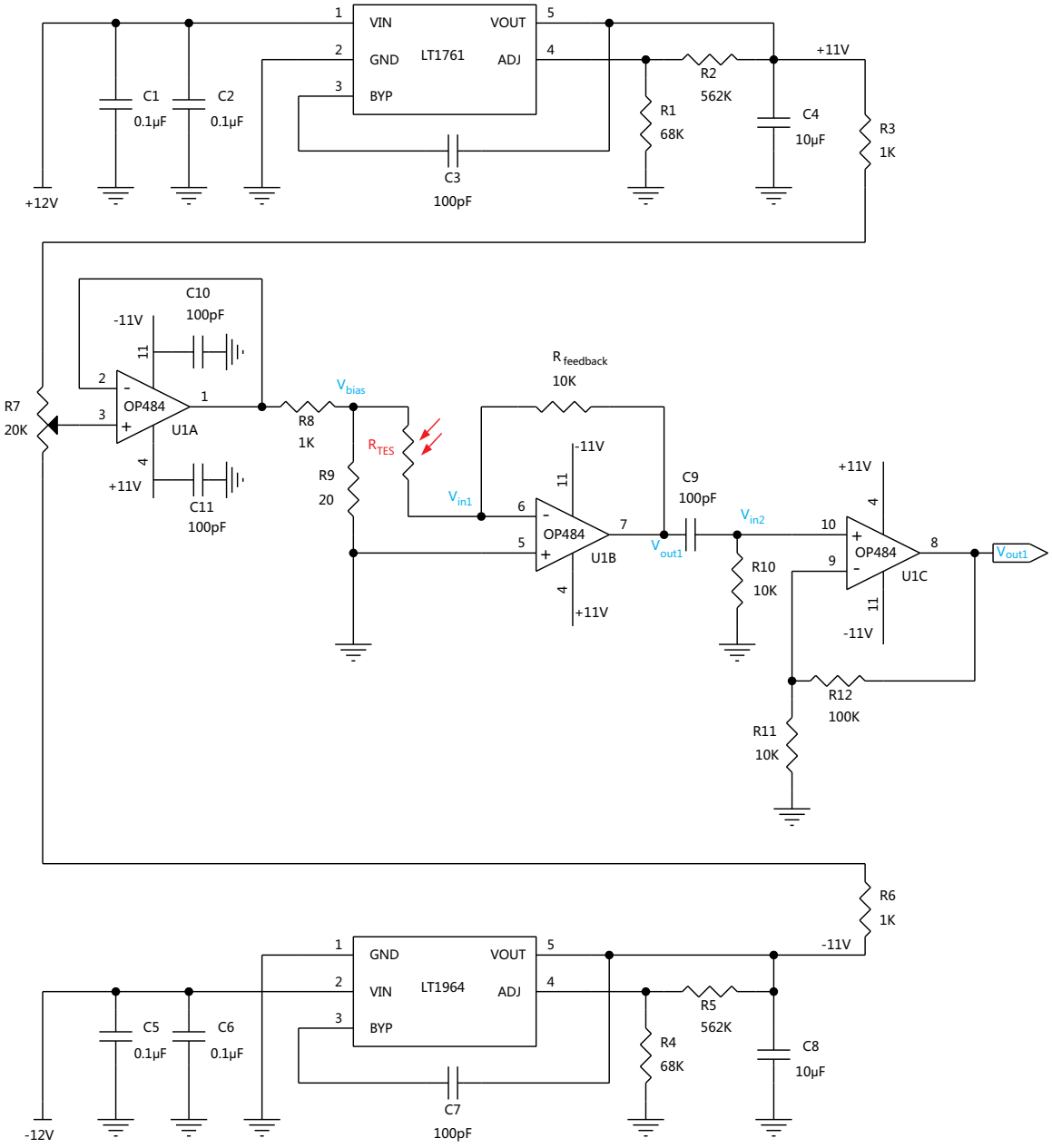

Figure A.2: Schematic of the TES preamplifier circuit for one channel.

The gain of the first-stage inverting amplifier is given by:

$$\frac{V_{out1} - V_{in1}}{R_{feedback}} = \frac{V_{in1} - V_{bias}}{R_{TES}}. \tag{A.1}$$

$$\because \quad V_{in1} = 0,$$

$$\begin{aligned} \therefore \quad G_1 &= \frac{V_{out1}}{V_{bias}} \\ &= -\frac{R_{feedback}}{R_{TES}} \\ &= -\frac{10^4}{R_{TES}}. \end{aligned} \tag{A.2}$$

The gain of the second-stage non-inverting amplifier is given by:

$$\begin{aligned} G_2 &= \frac{V_{out2}}{V_{in2}} \\ &= \frac{R_{11} + R12}{R_{11}} \\ &= 10. \end{aligned} \tag{A.3}$$

Therefore, the total gain of the preamplifier circuit is:

$$\begin{aligned} G &= G_1 \times G_2 \\ &= -\frac{10^5}{R_{TES}}. \end{aligned} \tag{A.4}$$

The performance of the circuit is considerably satisfying for our current stage of testing, but its defects should also be noticed. As the circuit works at room temperature of 300 K, Johnson noise of $\sqrt{4KT_{300K}R_{eq}}$ is not negligible, where R_{eq} is the equivalent impedance of the preamplifier circuit. Another limitation is the fluctuation of bias voltage

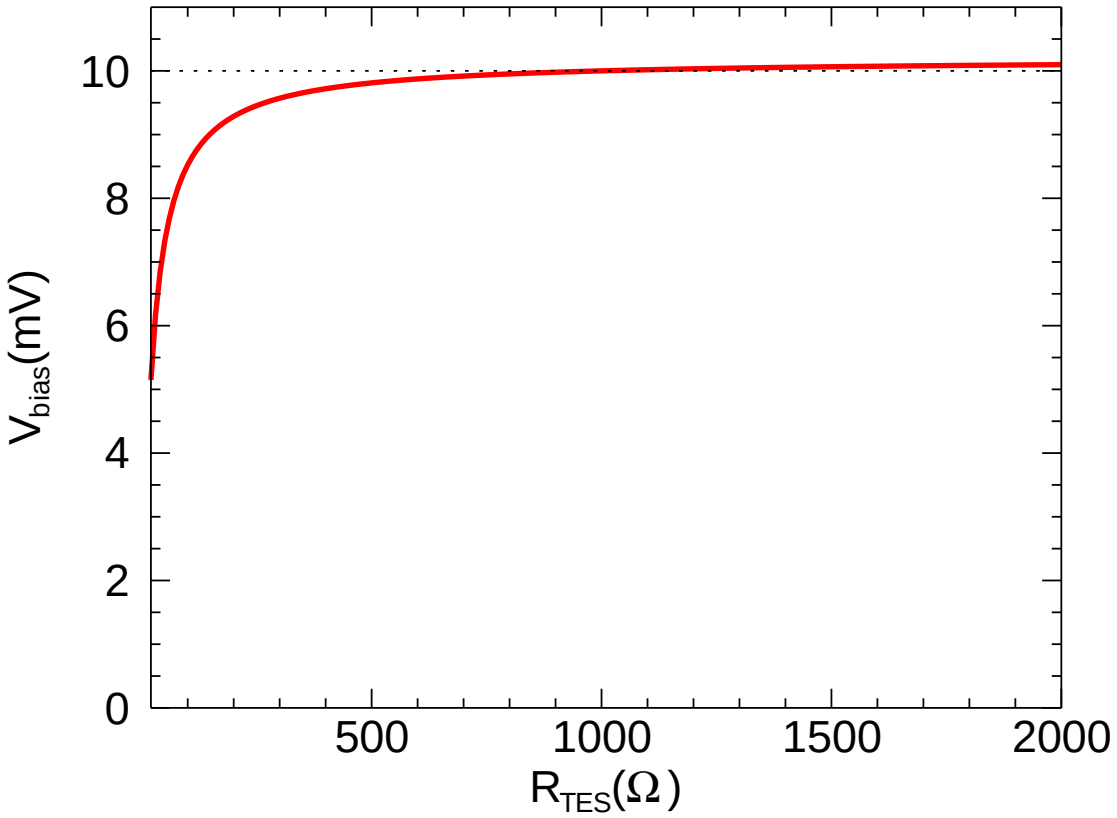

Figure A.3: V_{bias} is almost flat while the resistance of the TES is much higher than the resistance of the shunt resistor, but drops quickly at low TES resistance region.

V_bias caused by the simple shunt circuit. The shunt effect to maintain a constant V_{bias} works well only when the operating resistance of the TES is much higher than the shunt resistor, but for operating points close to the superconducting end of the transition V_{bias} has been observed to deviate from 10 mV. Figure A.3 shows this dependence of bias voltage on TES.

A better alternative is a transformer-coupled circuit (Figure A.4), where V_{in} is an AC voltage power, L_p and L_s are the inductance for the primary and secondary loops

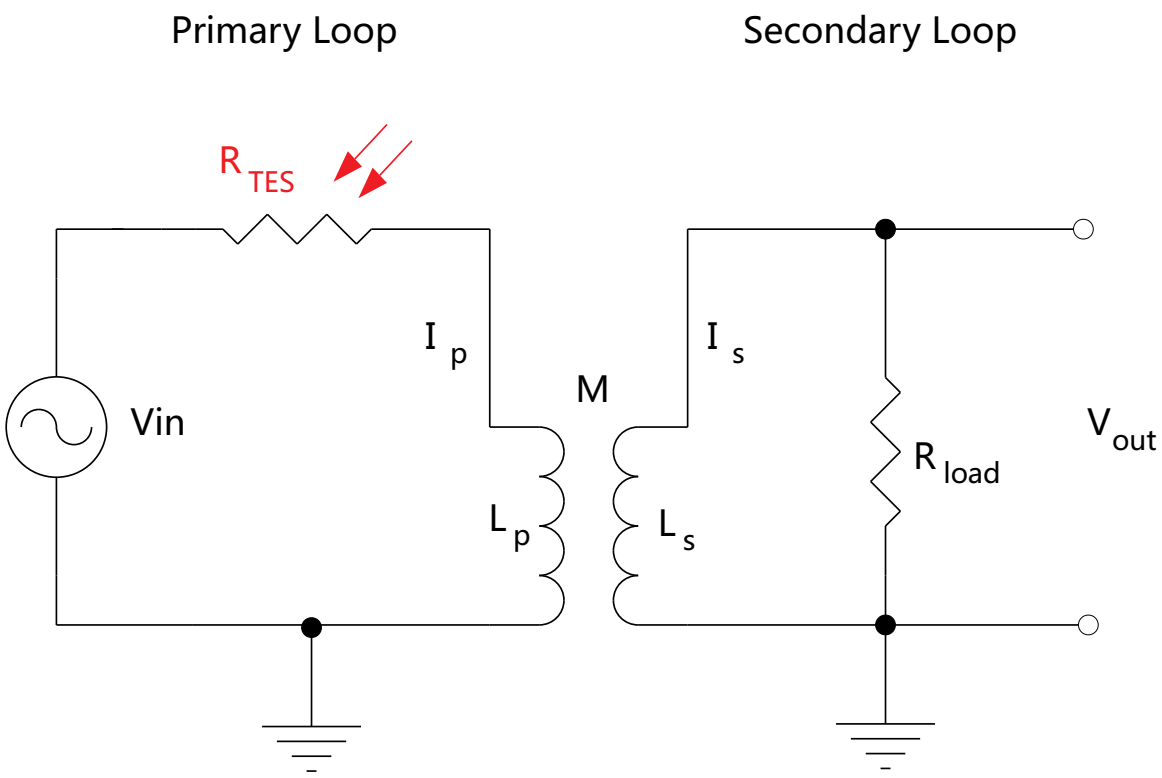

Figure A.4: Schematic of a transformer-coupled readout circuit.

respectively, M is the mutual inductance, and R_{load} is a load resistor. We have built a testing circuit with electronic components of negligible cost and compared it to the op-amp circuit with the same TES detector at the same conditions. Table A.1 shows that the transformer-coupled circuit has significantly reduced the total NEP of detector. In future we will further improve its performance and then replace the op-amp circuit with it.

Table A.1: Comparison of measured NEP through the op-amp and transformer-coupled circuits.

Circuit	Heat Sink Temperature (K)	NEP ($pW/Hz^1/2$)
Op-amp	6.94	2.4
Transformer-coupled	6.94	0.53

Appendix B

Labview Code

Darren Hayton [53] programmed the following Labview code, and I helped to test them in detector performance experiments.

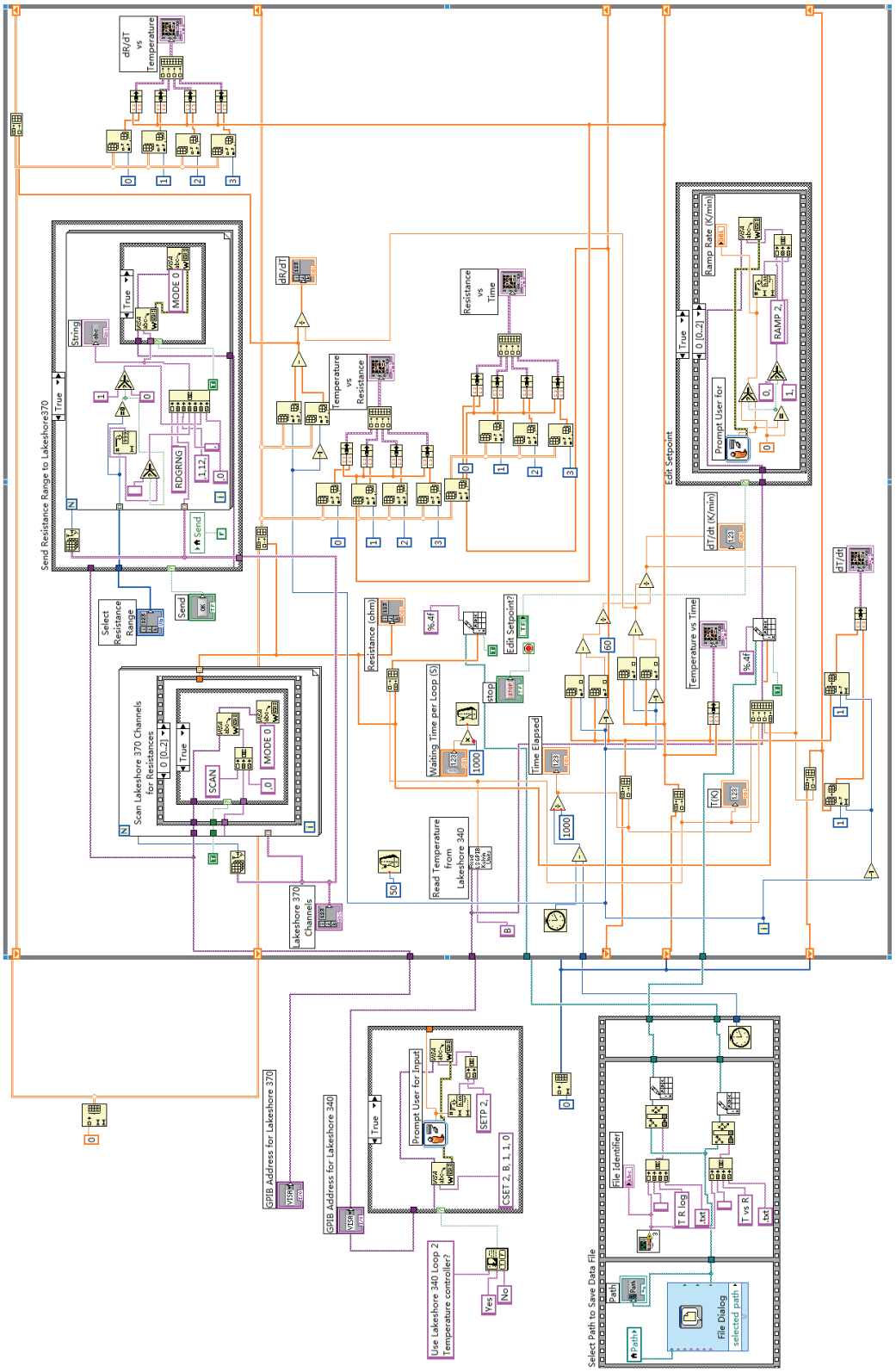

Figure B.1: Labview code for plotting temperature versus resistance curves via Lakeshore 340 temperature controller.

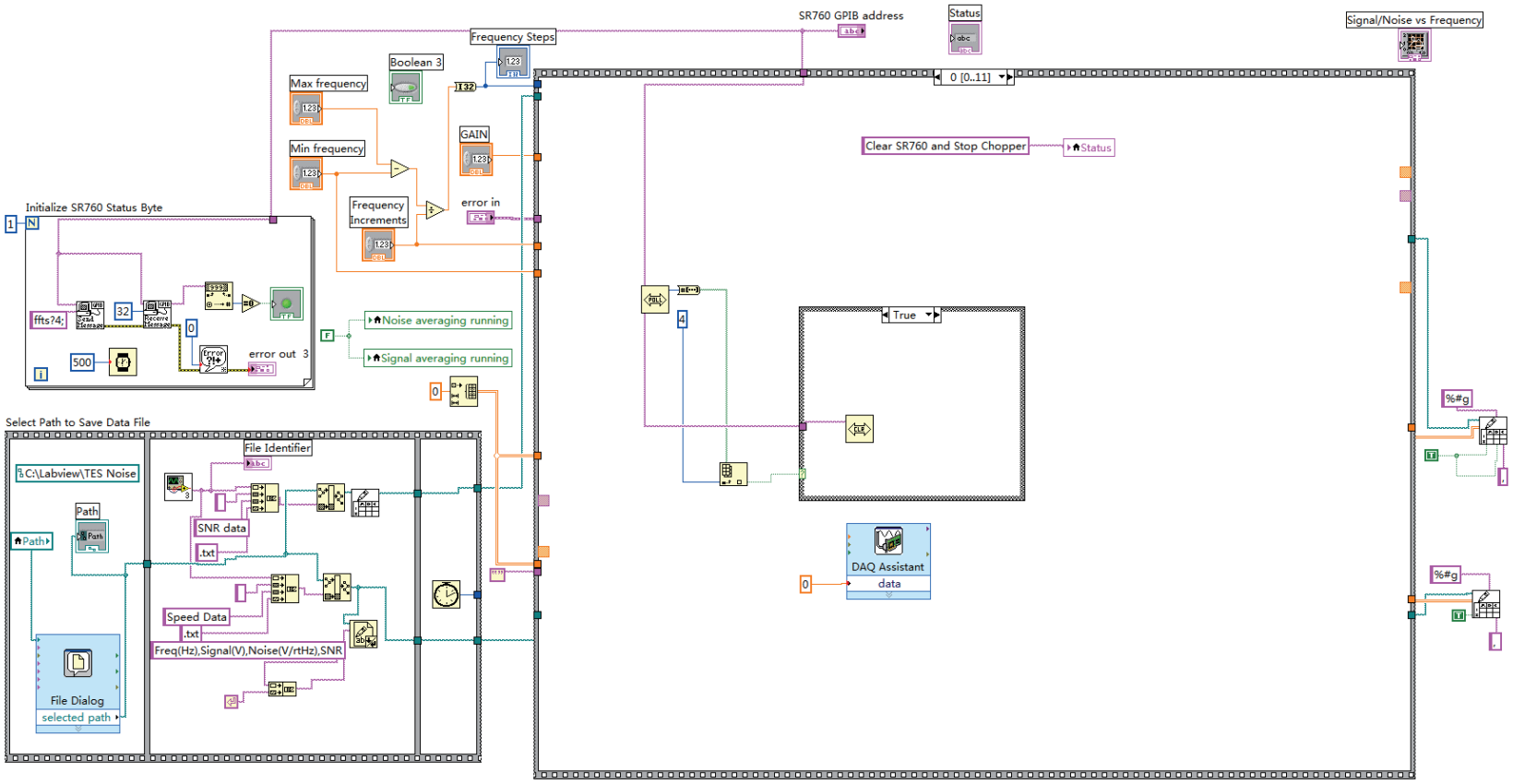

Figure B.2: Labview code for measuring NEP: step 0. clear the SR760 spectrum analyzer and stop the chopper.

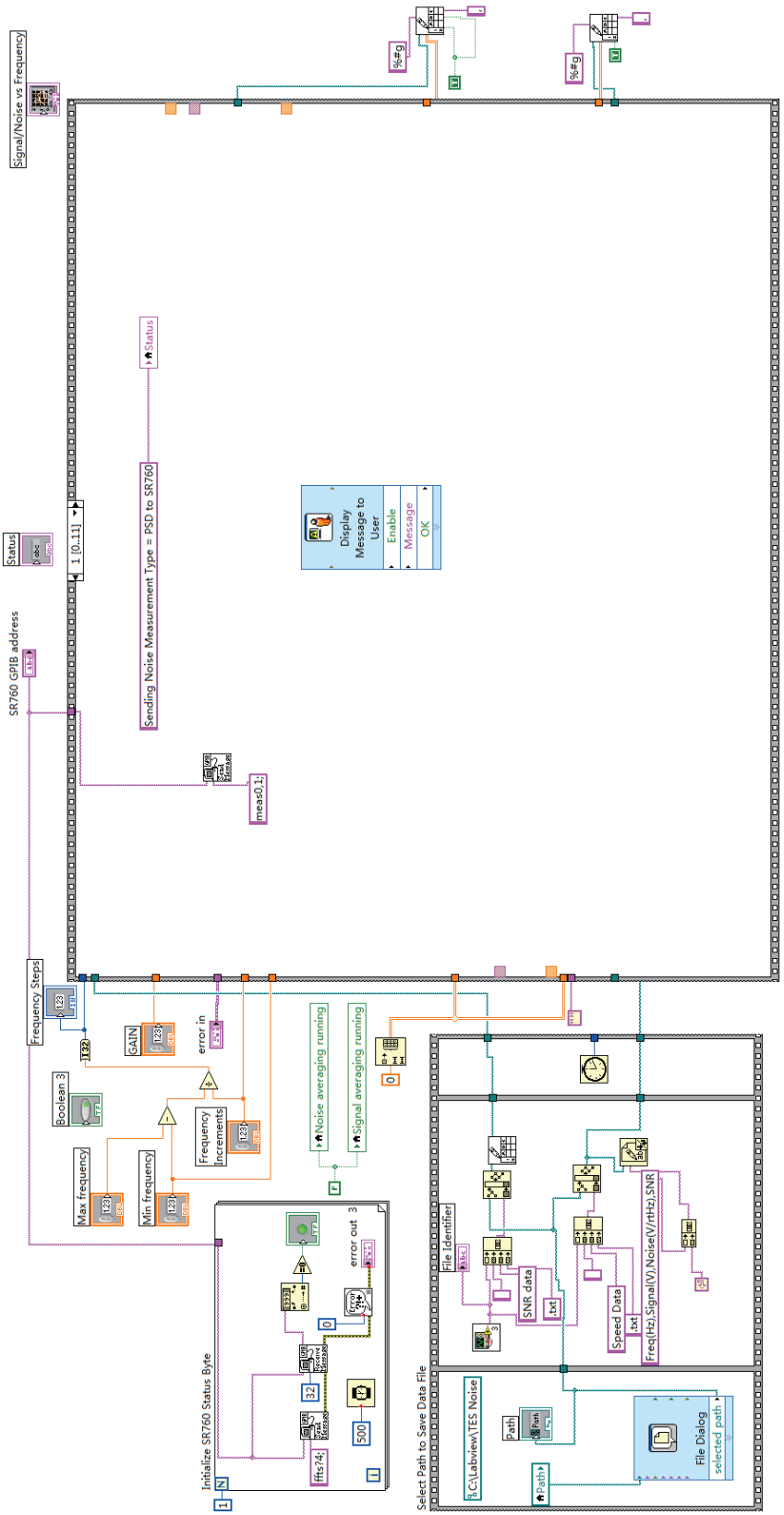

Figure B.3: Labview code for measuring NEP: step 1. sending noise measurement type of PSD (power spectral density) to the SR760 spectrum analyzer.

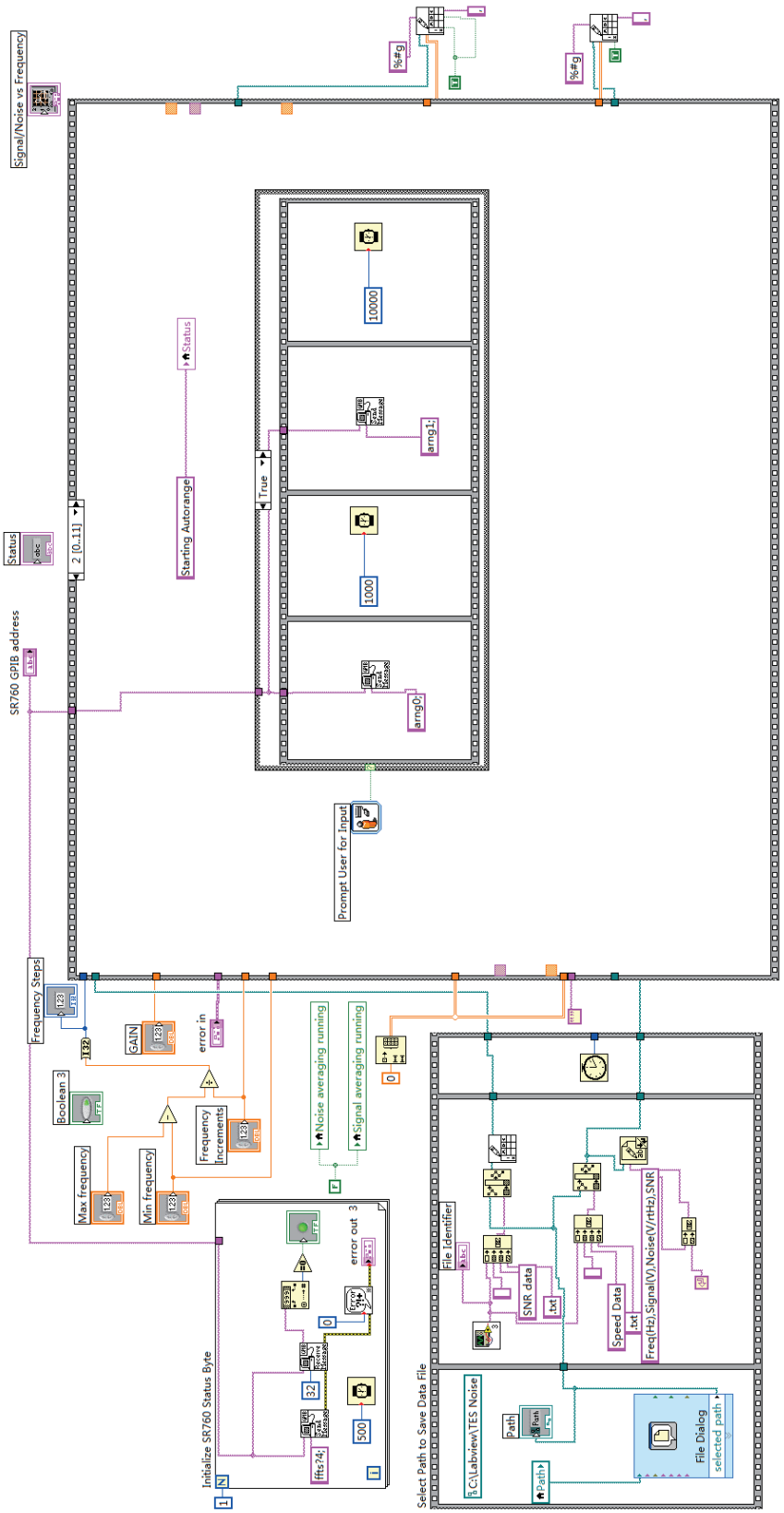

Figure B.4: Labview code for measuring NEP: step 2. starting autorange function on the spectrum analyzer.

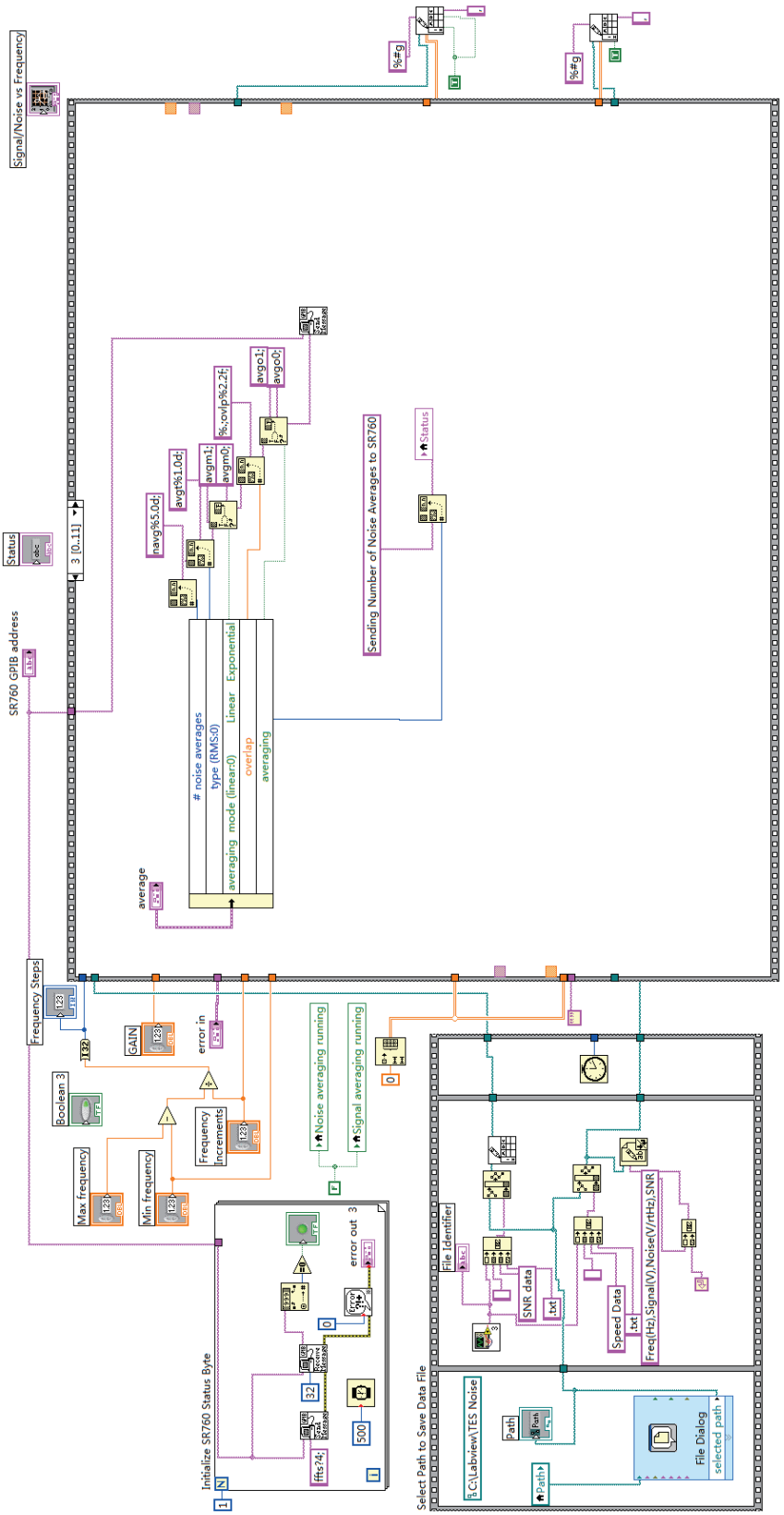

Figure B.5: Labview code for measuring NEP: step 3. sending number of noise averages to the spectrum analyzer.

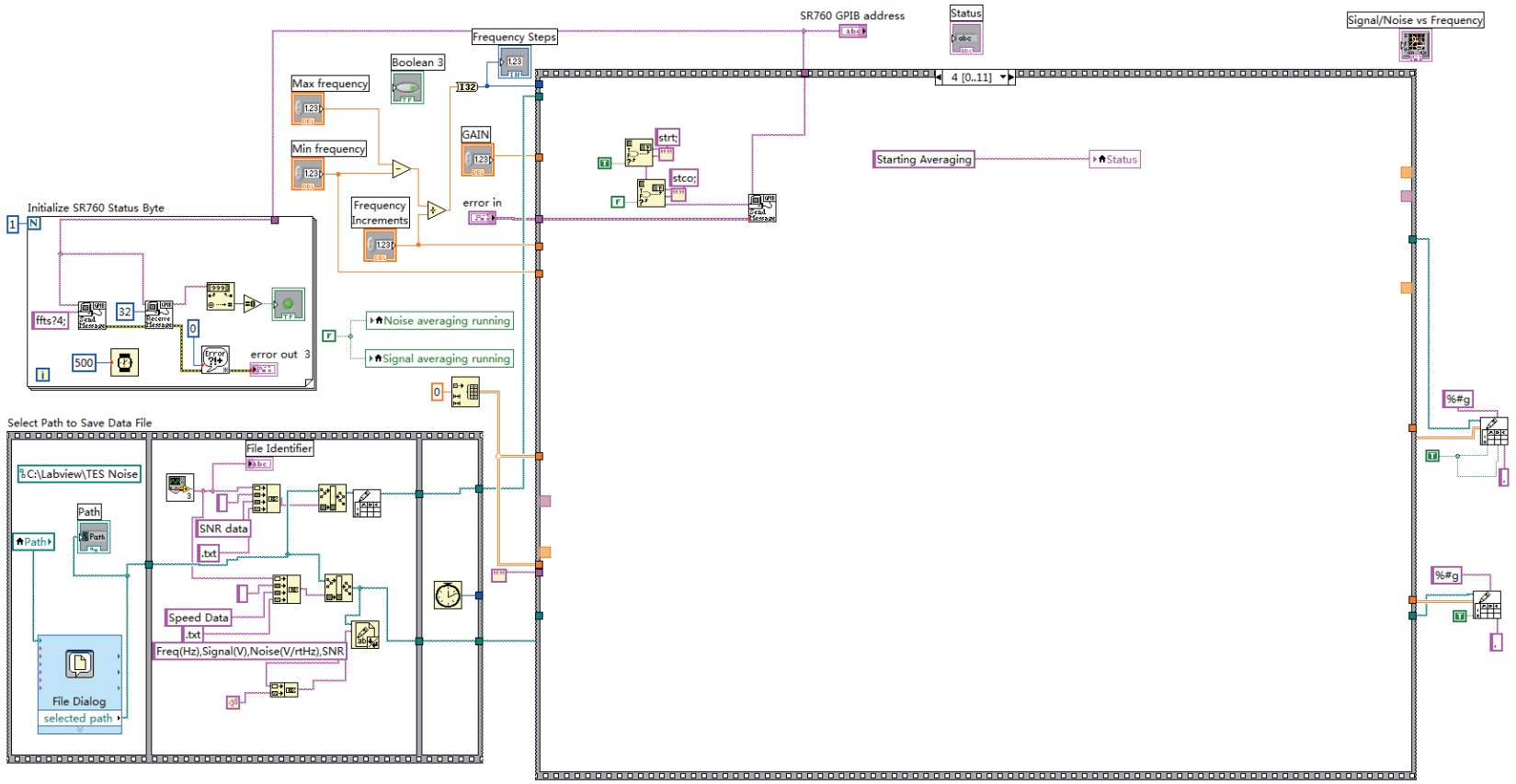

Figure B.6: Labview code for measuring NEP: step 4. starting noise averaging.

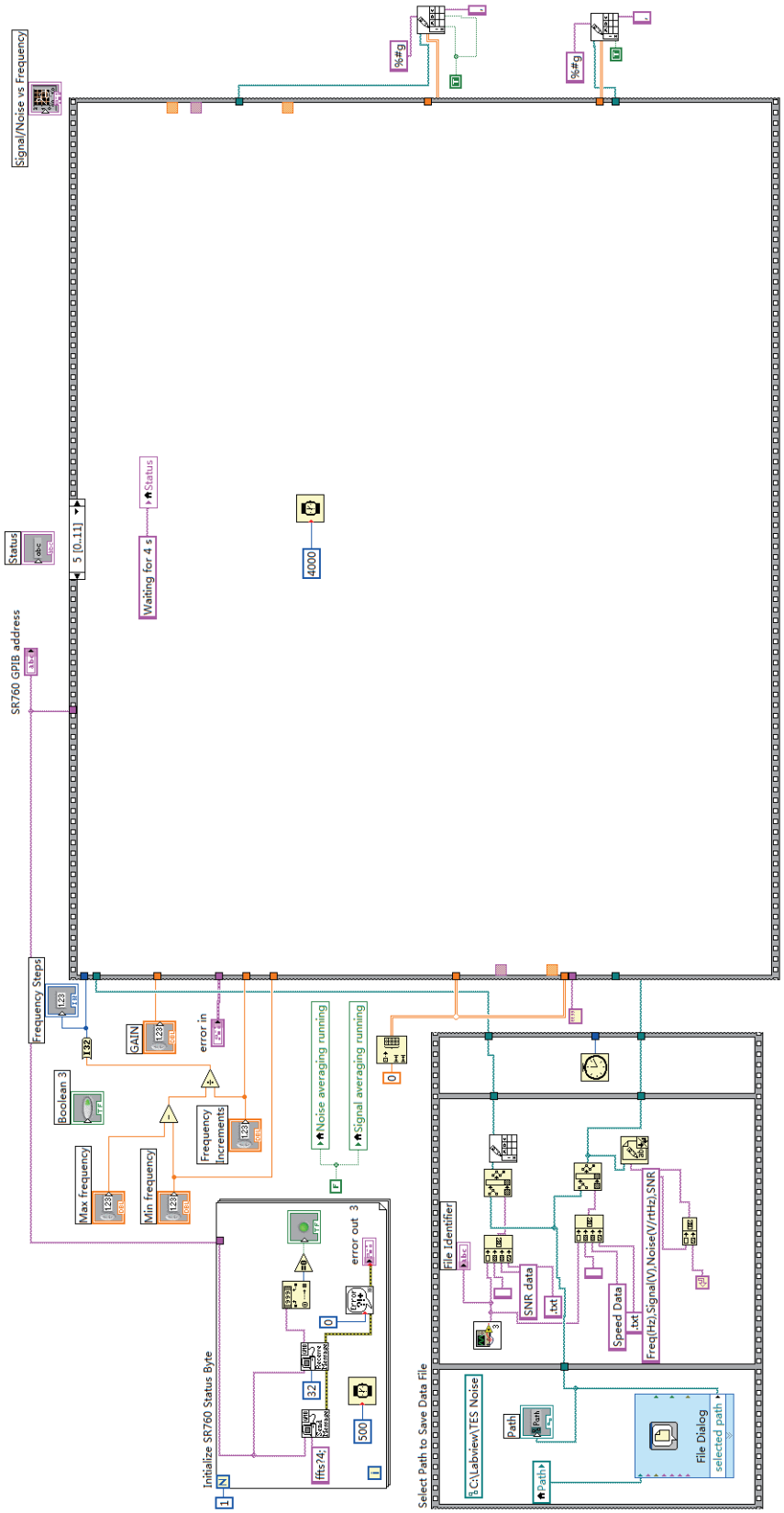

Figure B.7: Labview code for measuring NEP: step 5. waiting for 4 s.

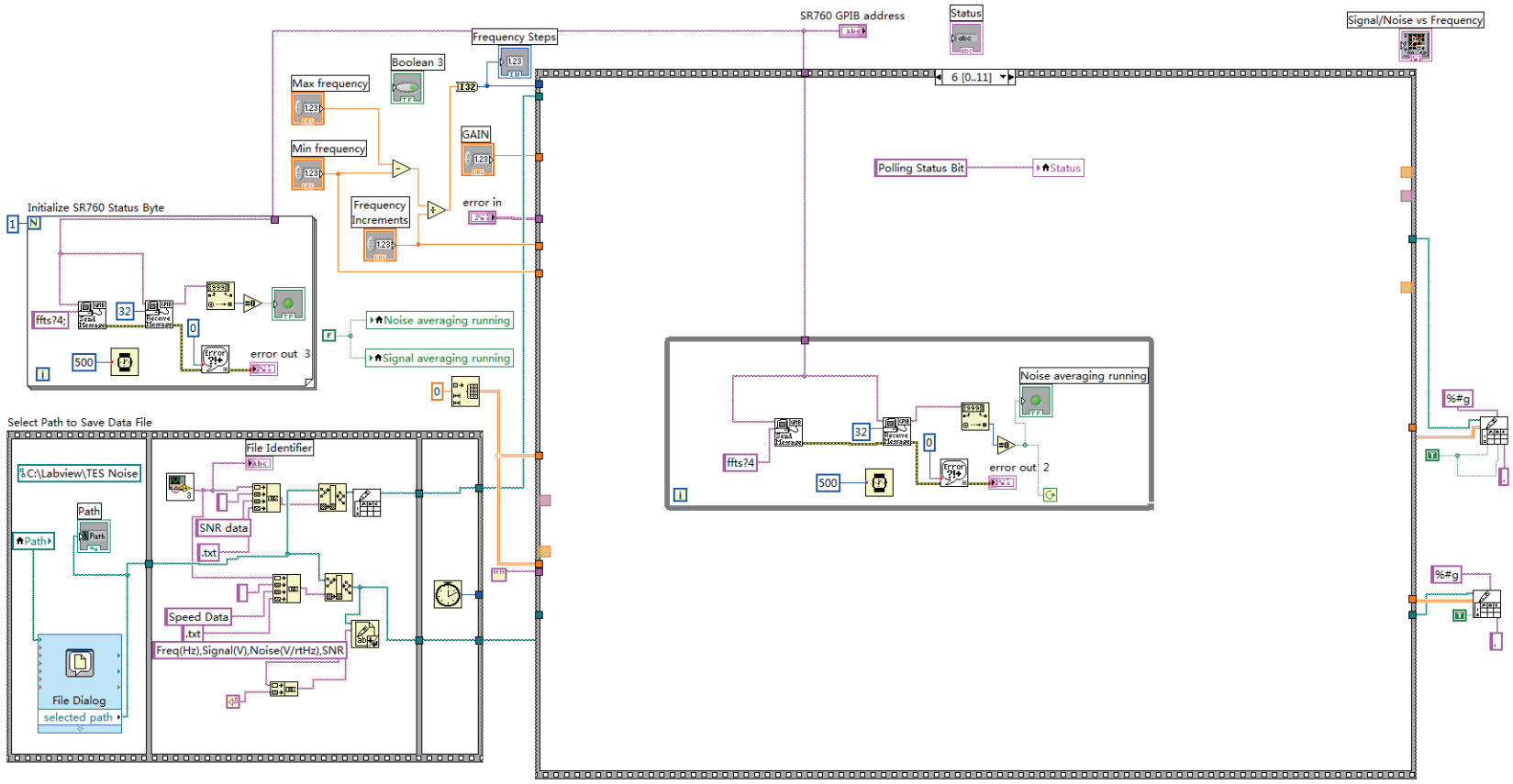

Figure B.8: Labview code for measuring NEP: step 6. polling status bit from the spectrum analyzer.

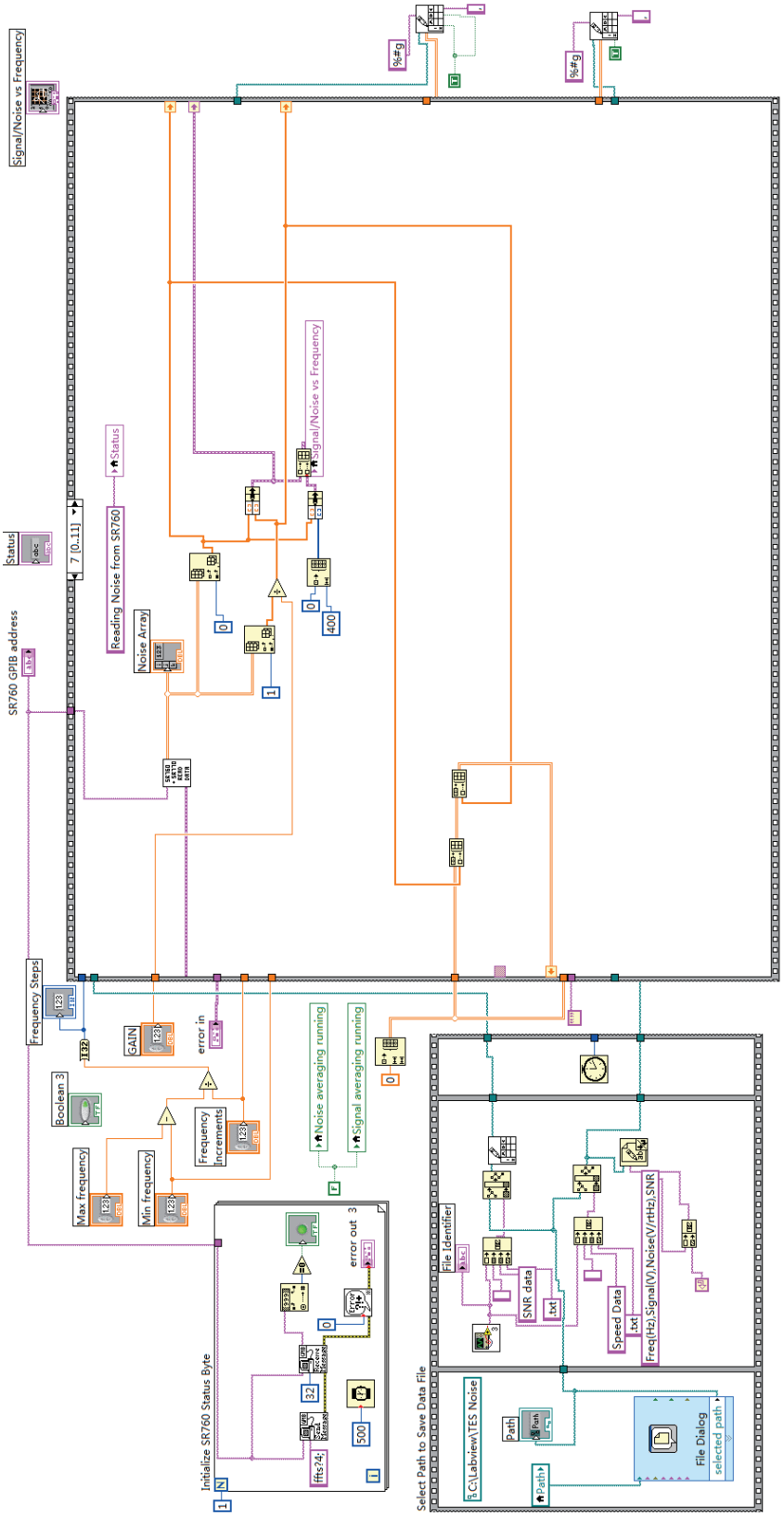

Figure B.9: Labview code for measuring NEP: step 7. reading noise from the spectrum analyzer.

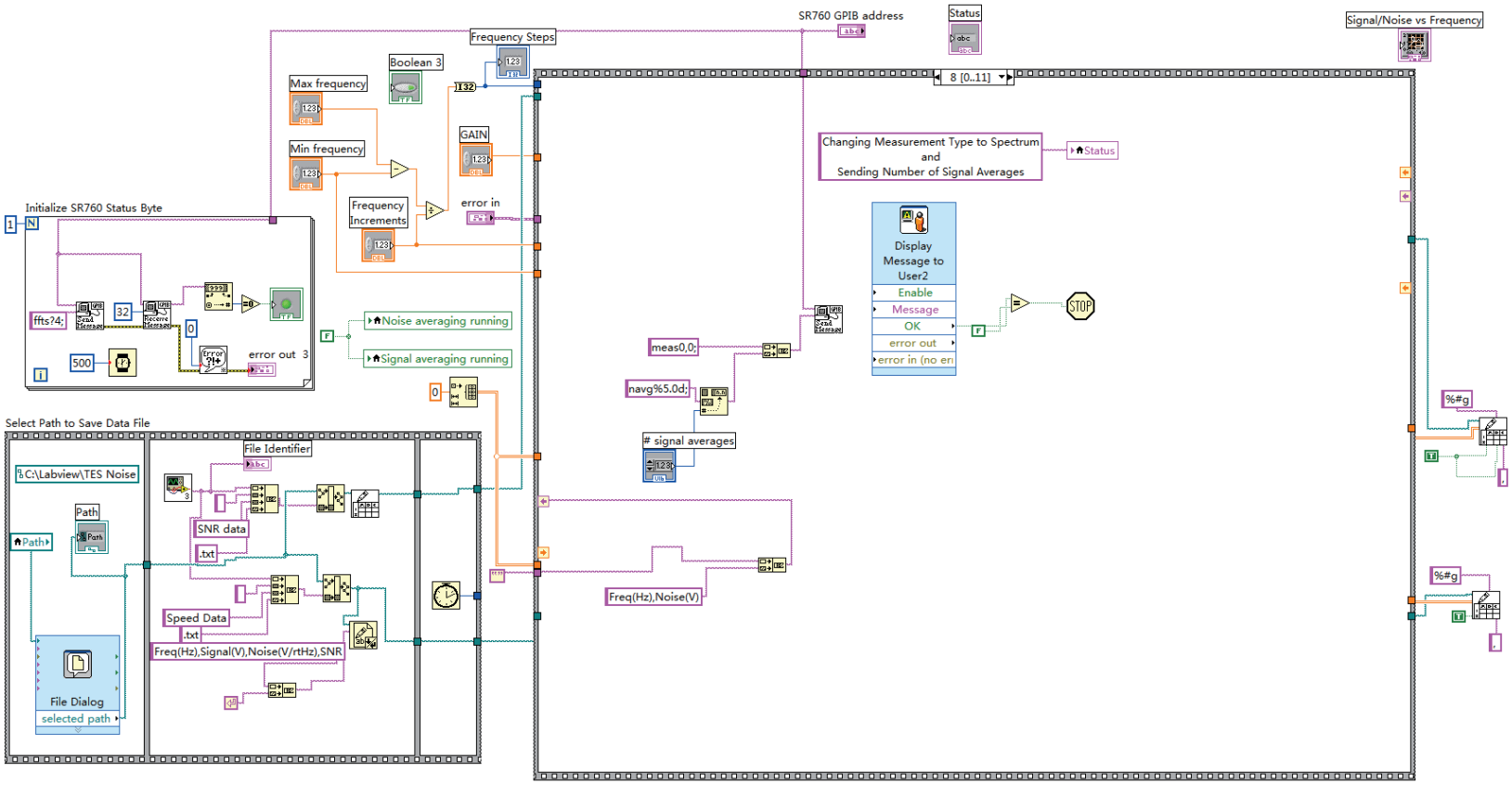

Figure B.10: Labview code for measuring NEP: step 8. changing signal measurement the type of spectrum and sending number of signal averages.

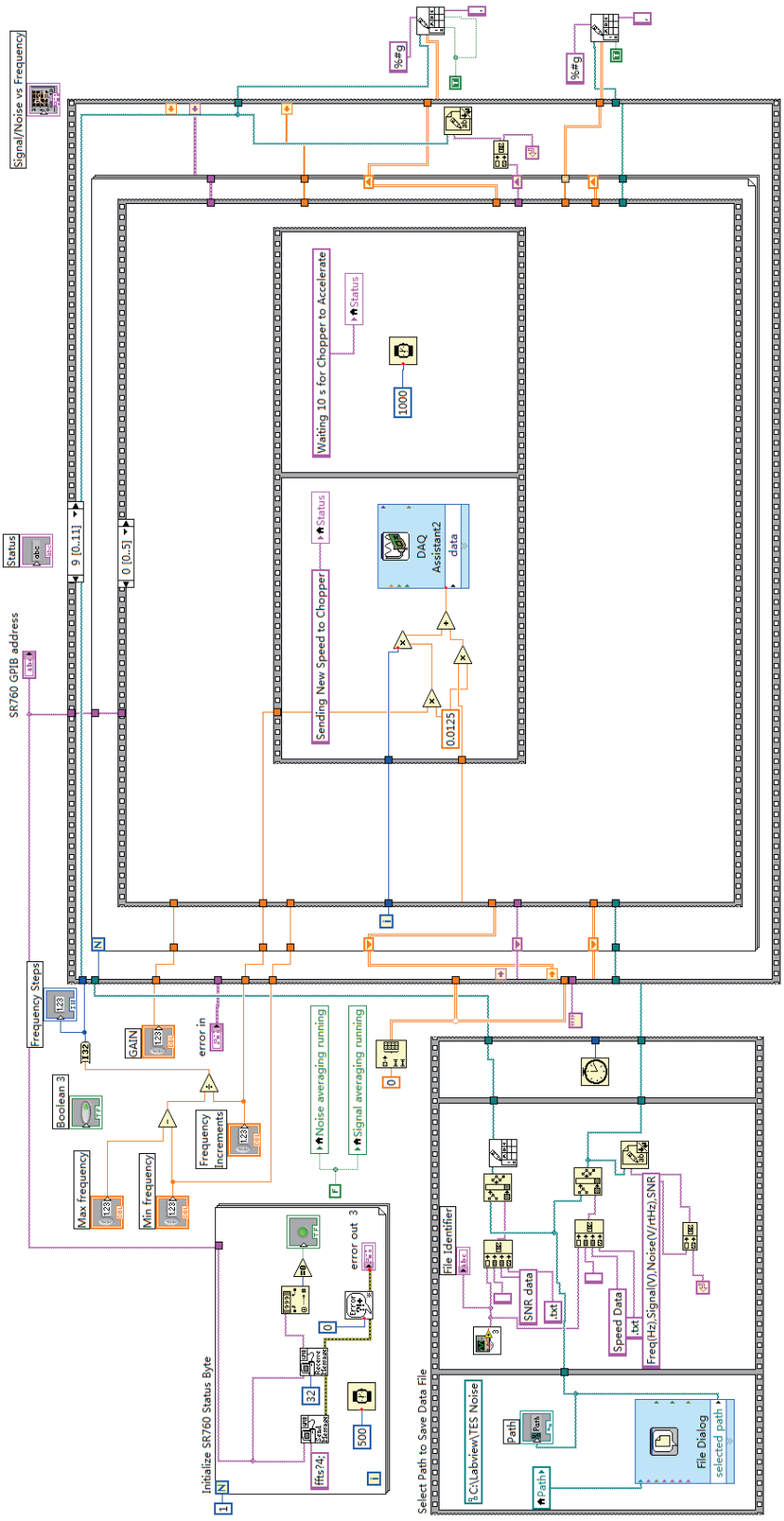

Figure B.11: Labview code for measuring NEP: step 9-0. sending new speed to the chopper and waiting 10 s for it to accelerate.

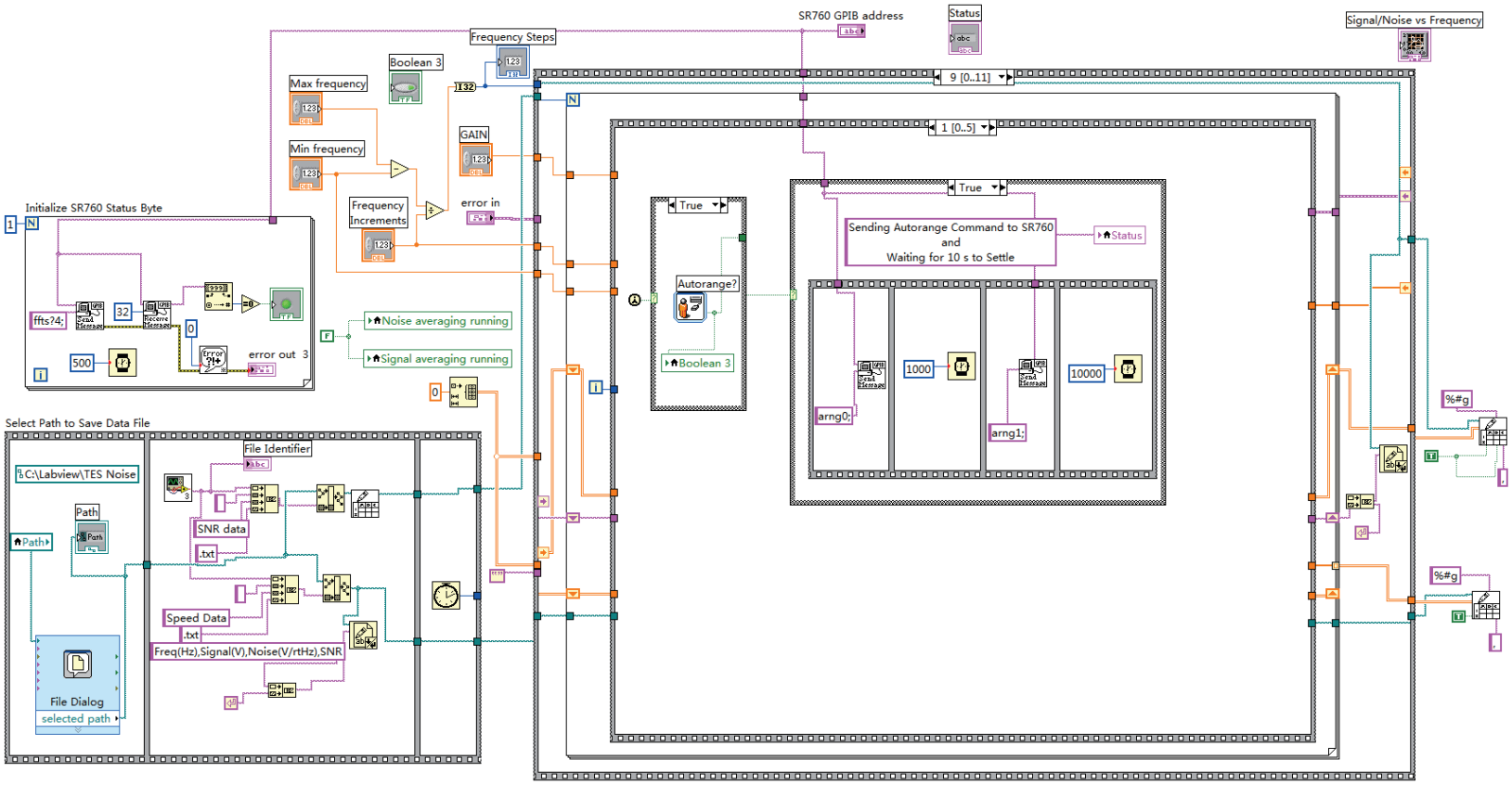

Figure B.12: Labview code for measuring NEP: step 9-1. sending autorange command to the spectrum analyzer and waiting for 10 s to settle.

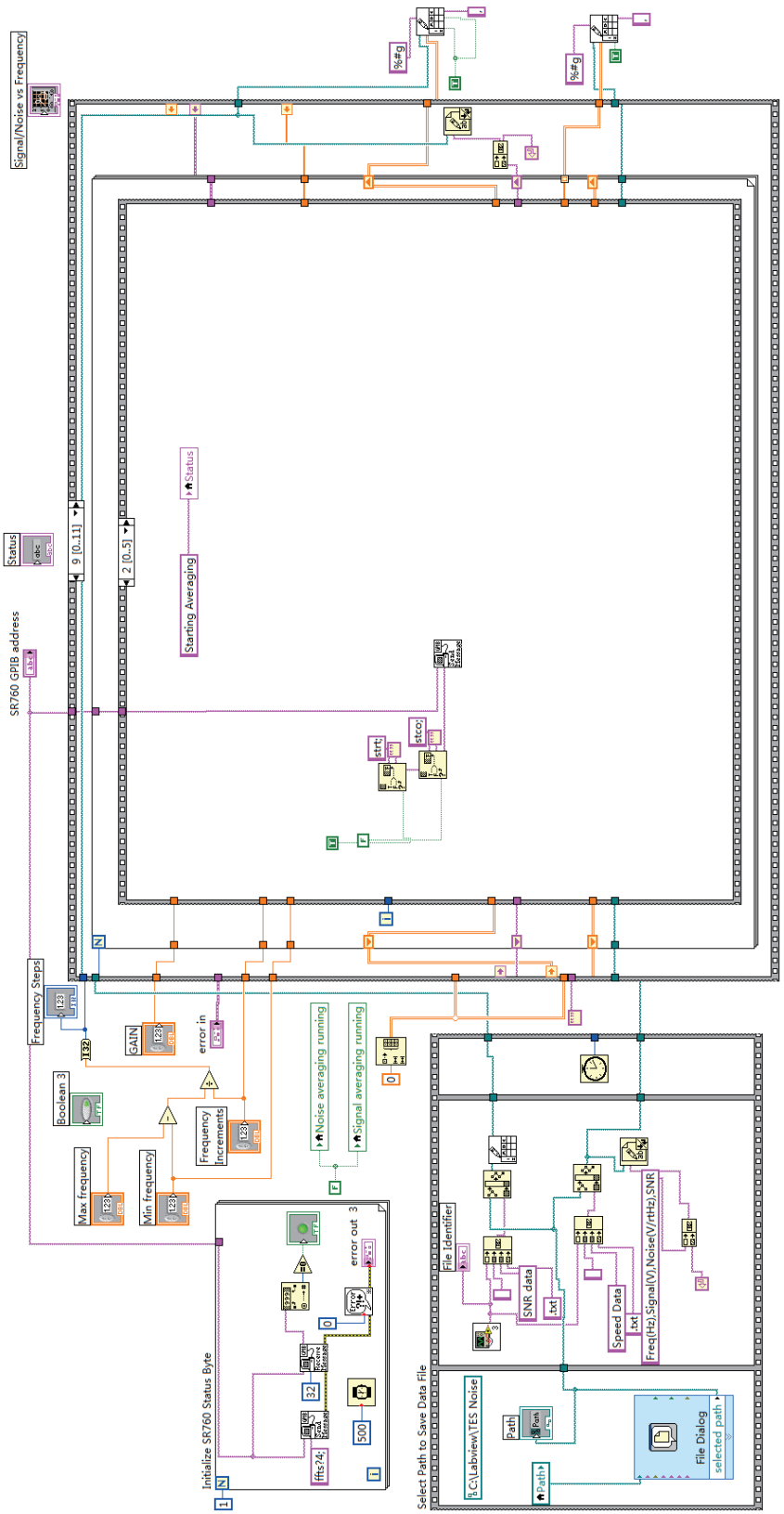

Figure B.13: Labview code for measuring NEP: step 9-2. starting signal averaging.

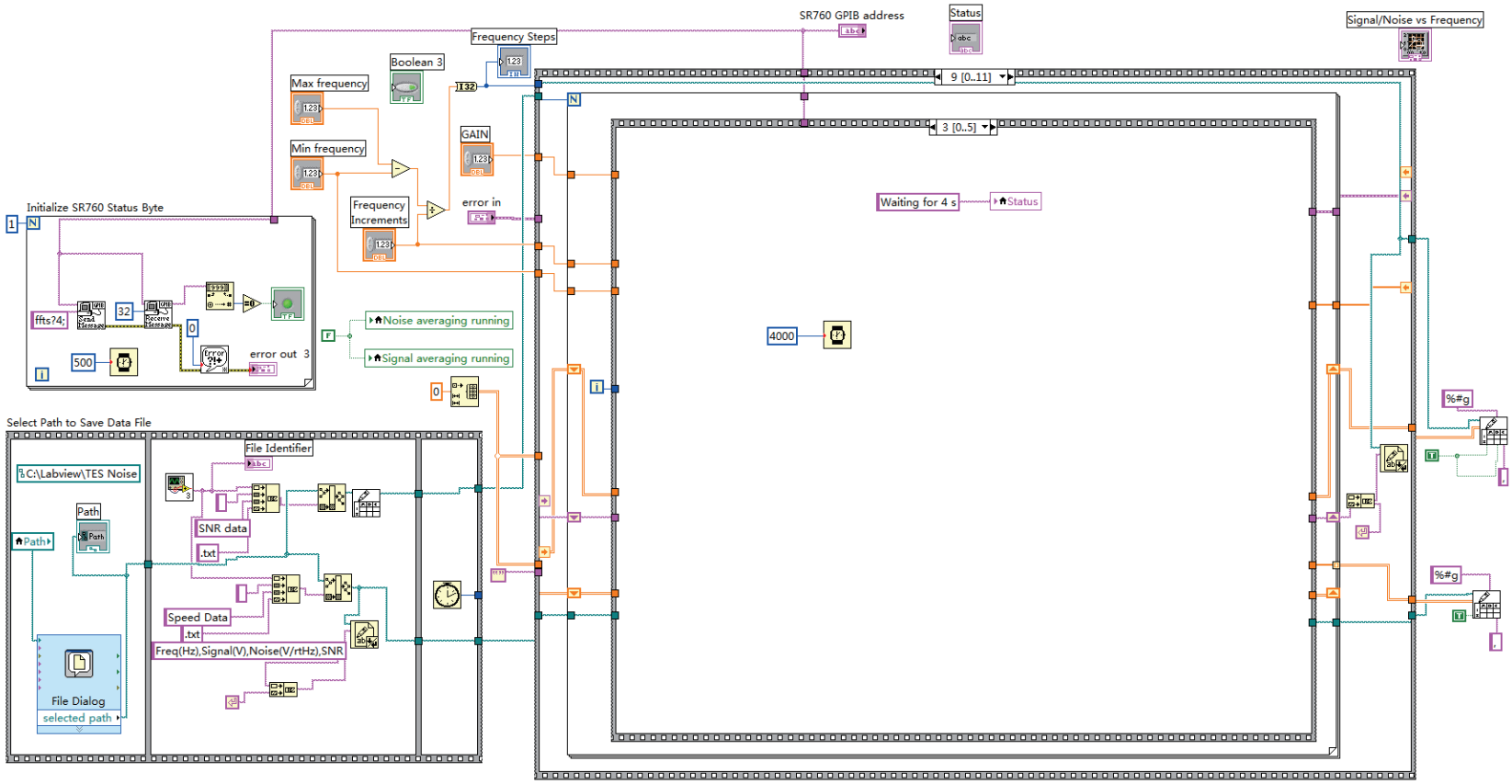

Figure B.14: Labview code for measuring NEP: step 9-3. waiting for 4 s.

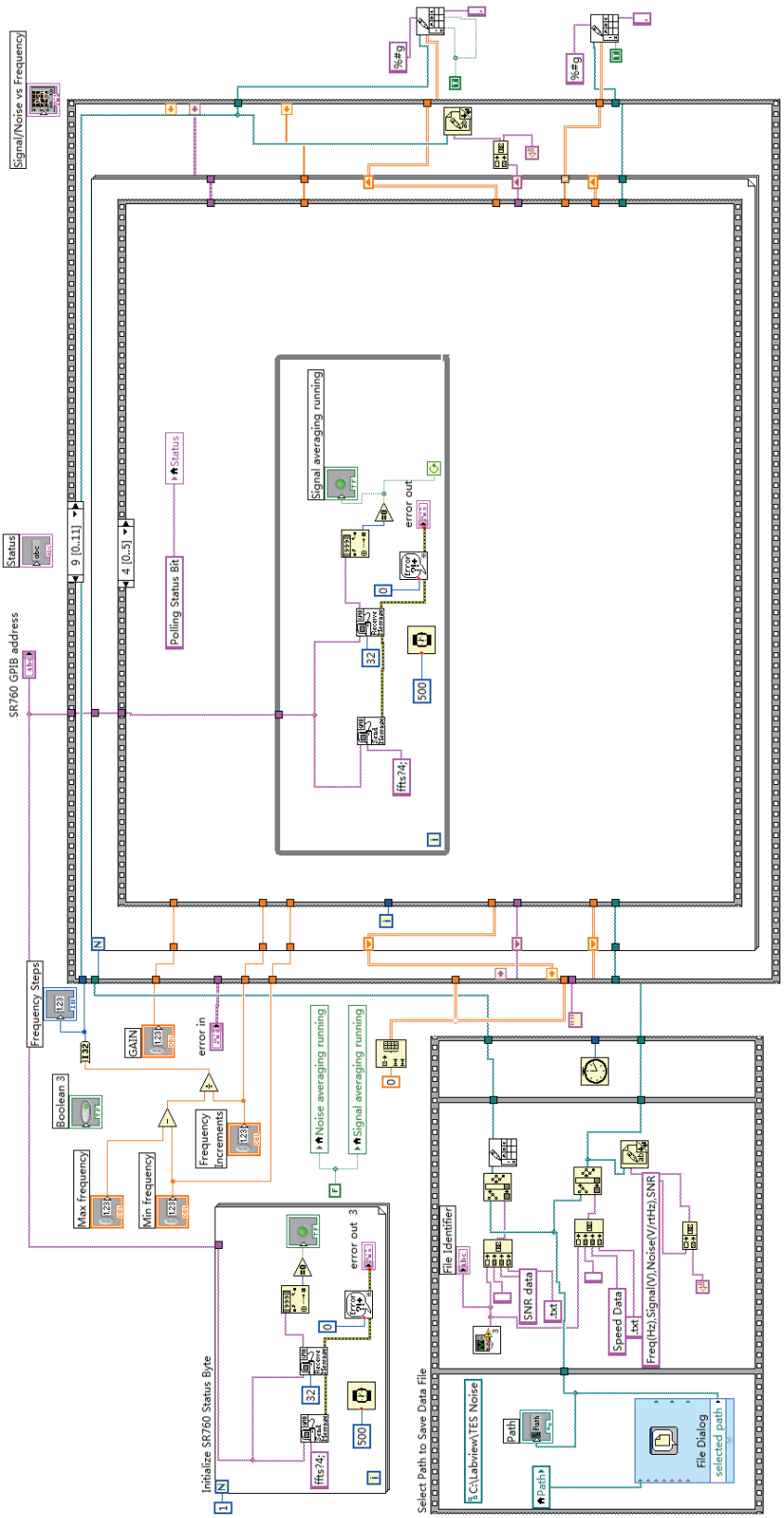

Figure B.15: Labview code for measuring NEP: step 9-4. polling status bit from the spectrum analyzer.

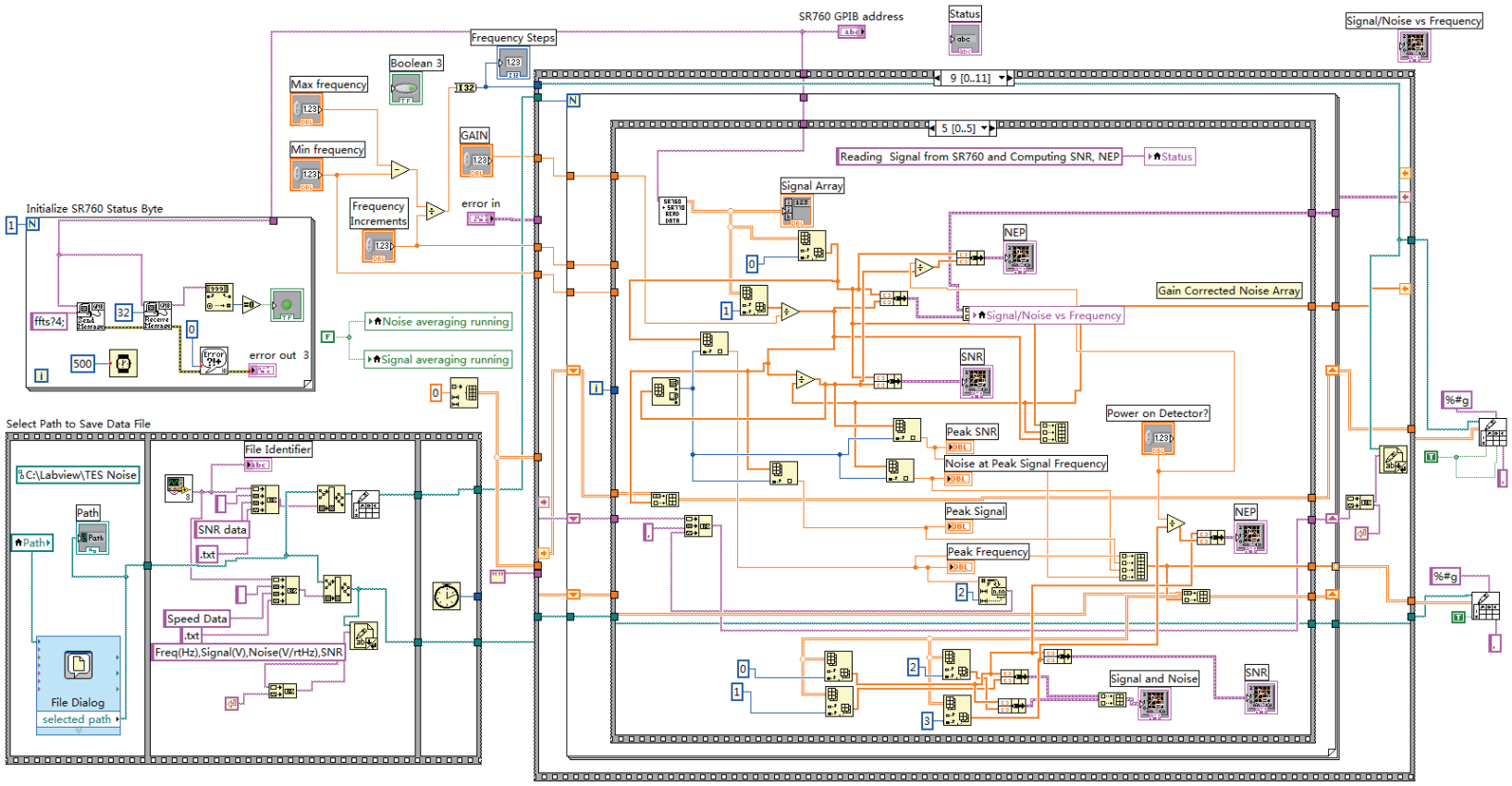

Figure B.16: Labview code for measuring NEP: step 9-5. reading signal from the spectrum analyzer and computing SNR, NEP.

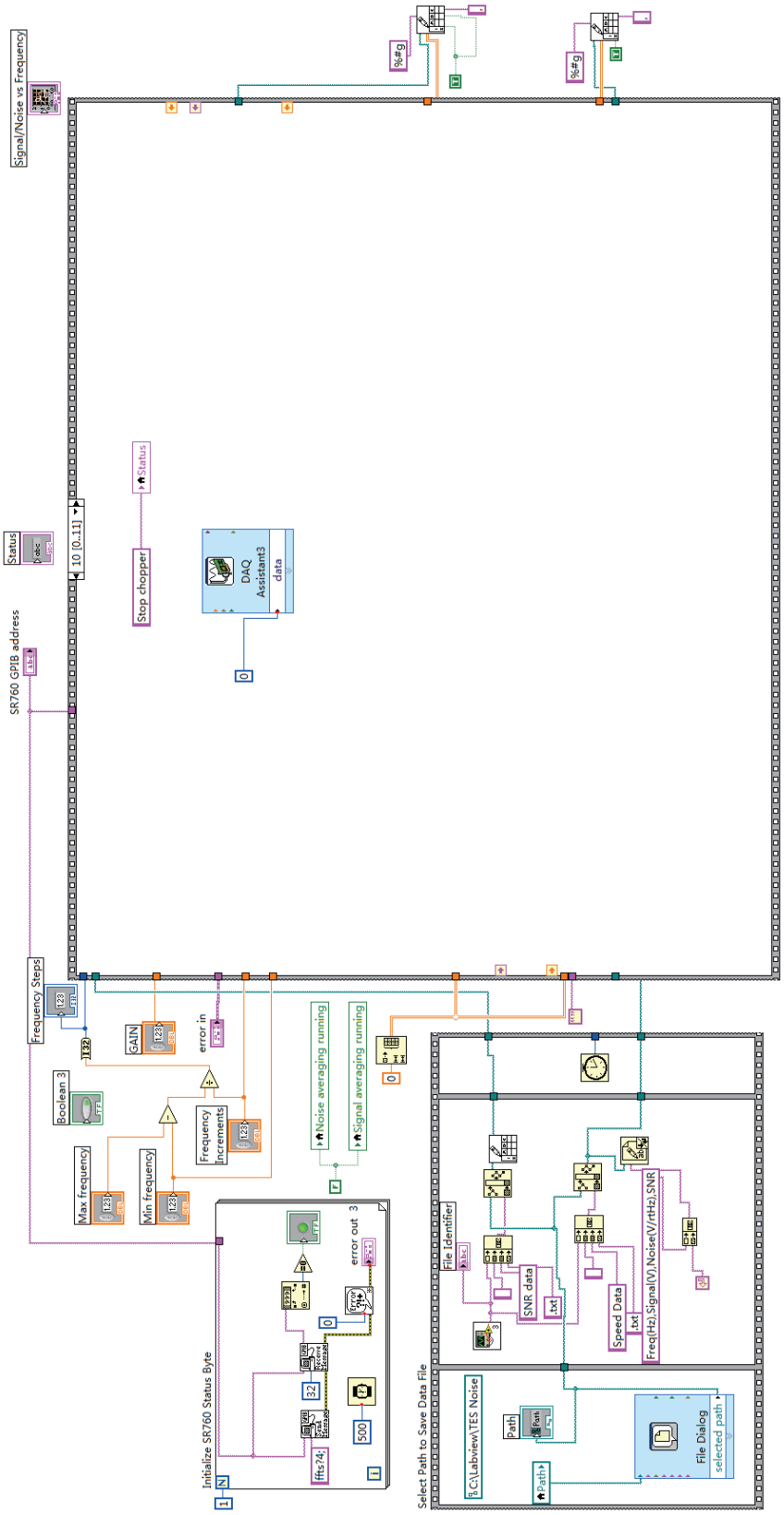

Figure B.17: Labview code for measuring NEP: step 10. stop the chopper.

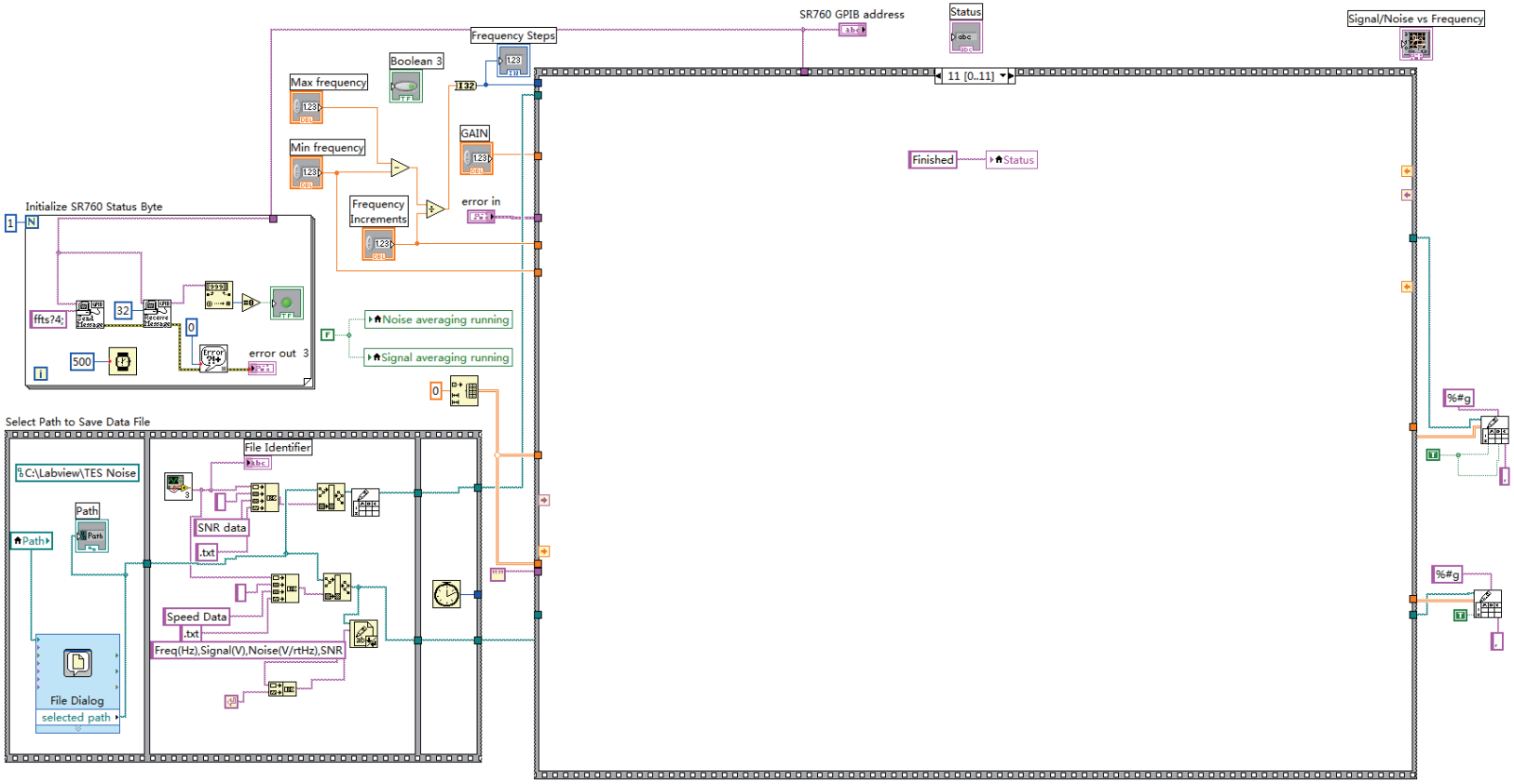

Figure B.18: Labview code for measuring NEP: step 11. measurements finish.

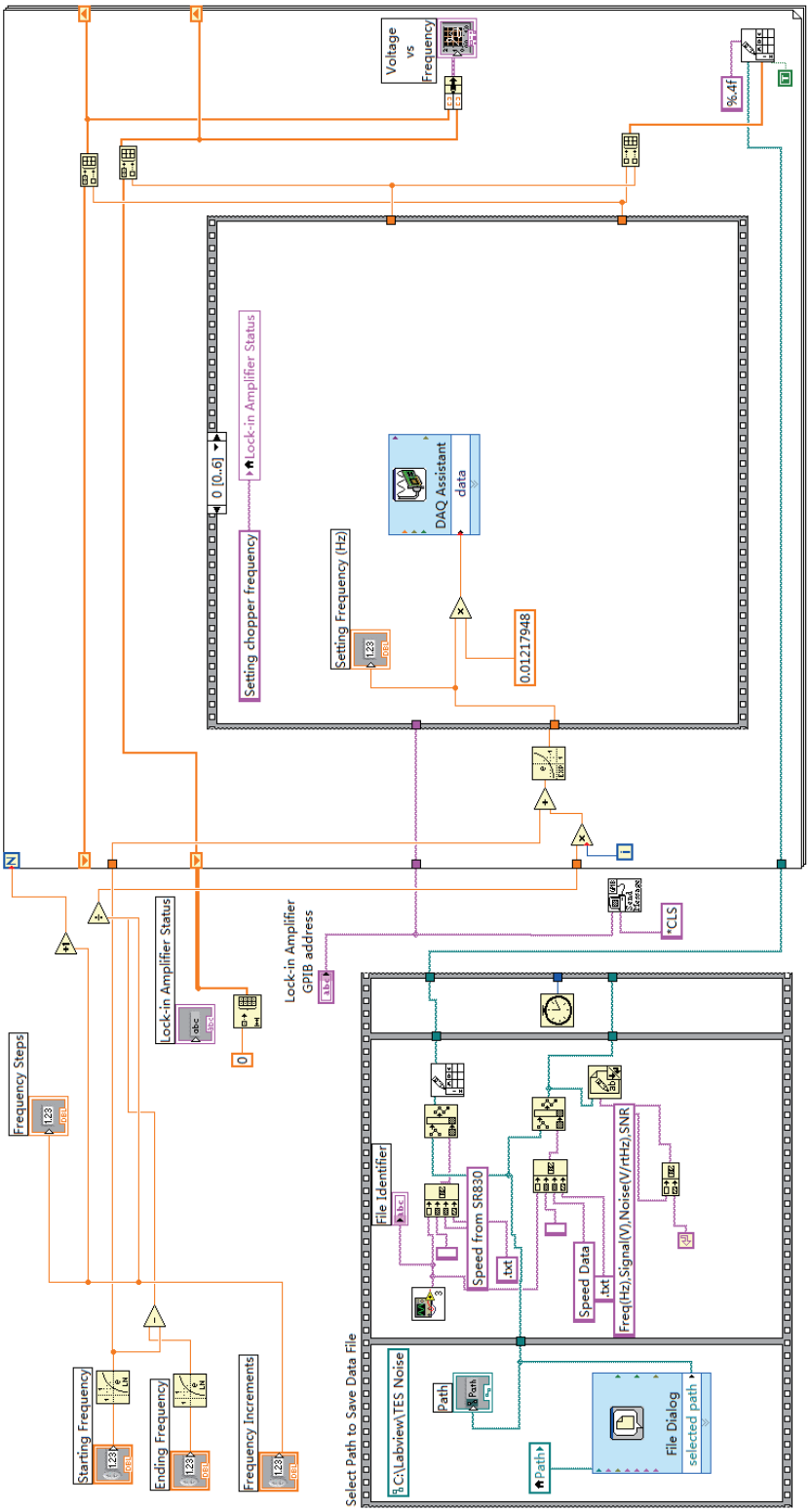

Figure B.19: Labview code for measuring frequency response: step 0. setting chopper frequency.

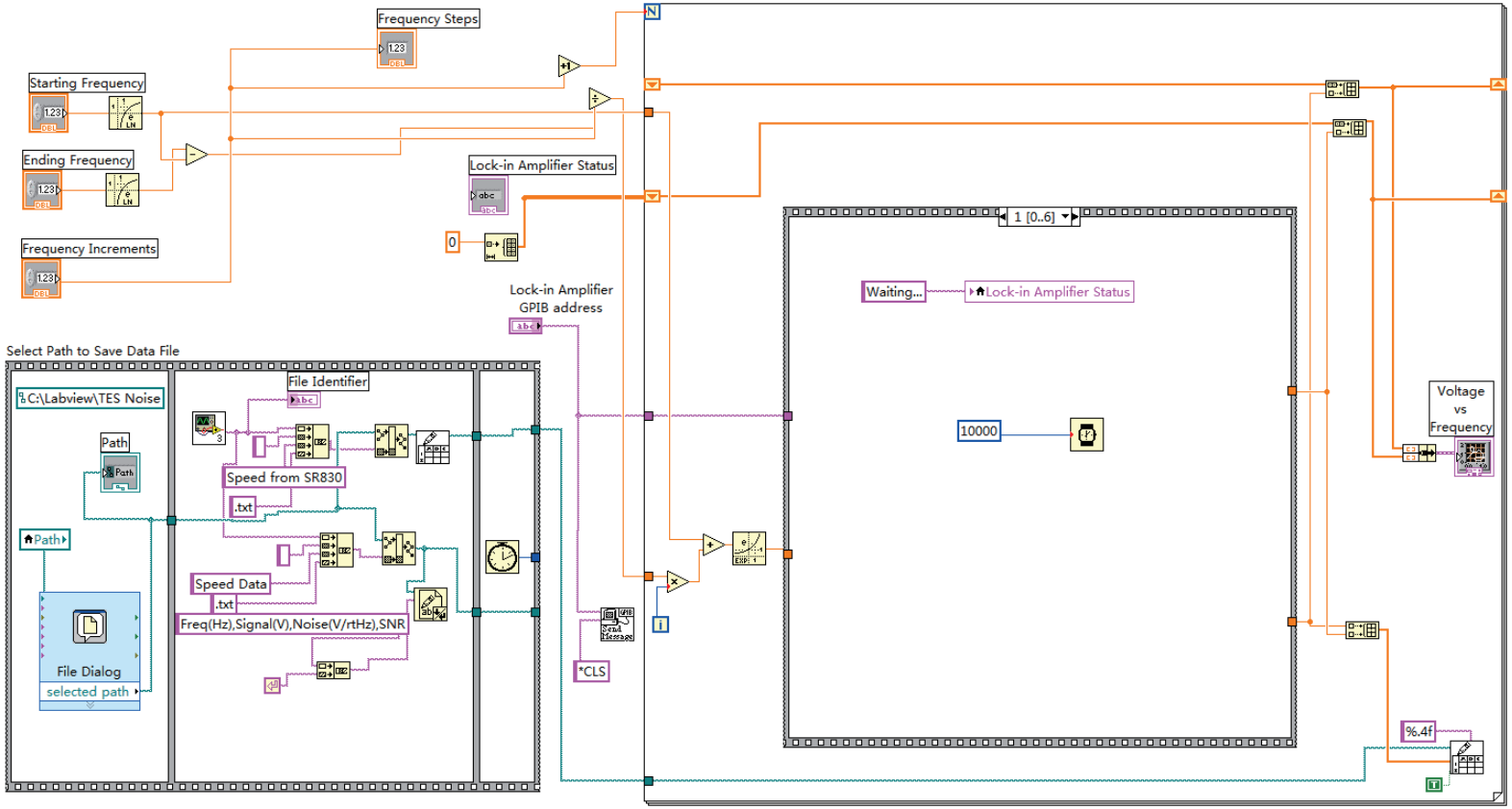

Figure B.20: Labview code for measuring frequency response: step 1. waiting for 10 s.

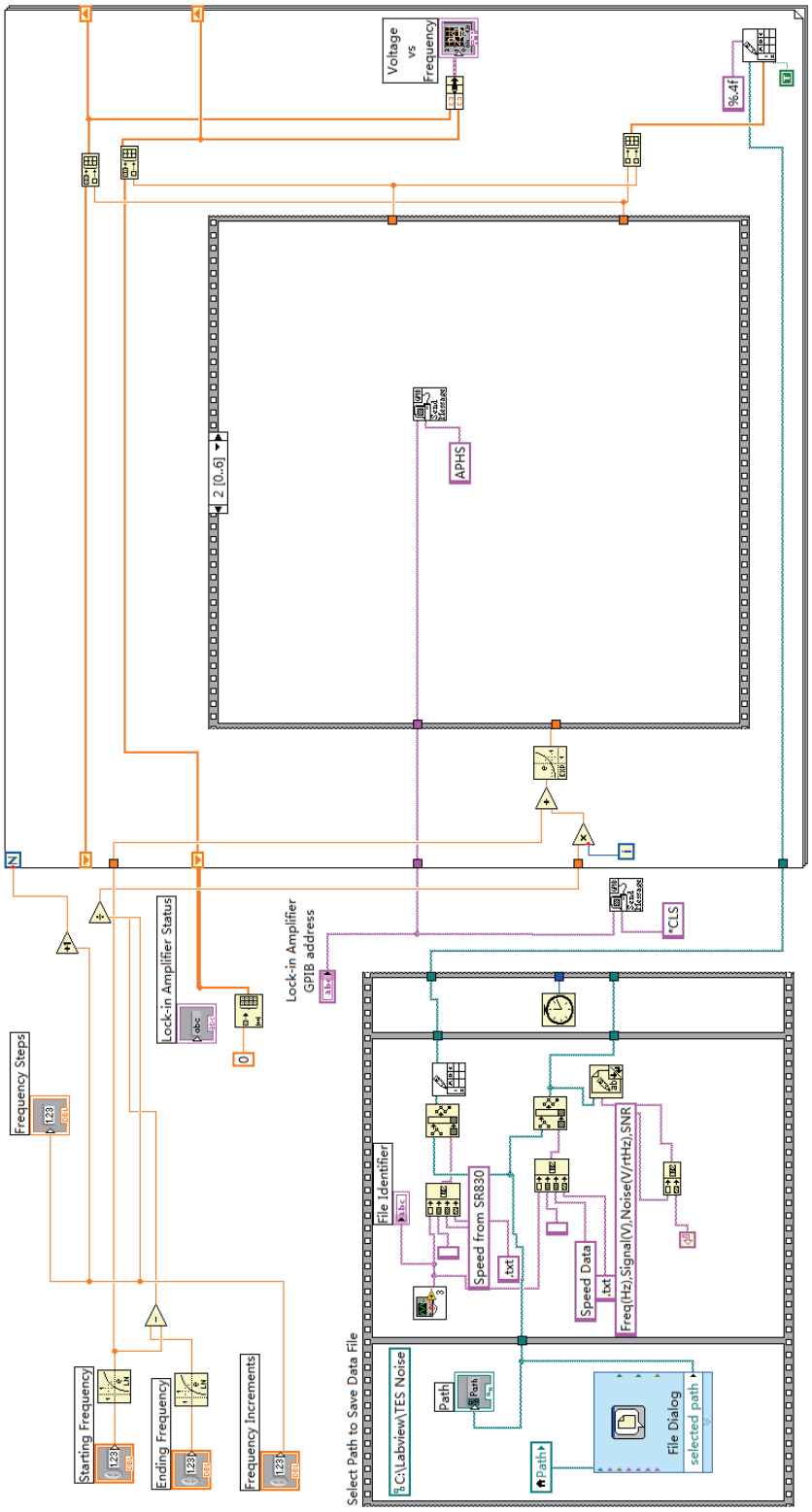

Figure B.21: Labview code for measuring frequency response: step 2. automatically adjust the reference phase shift to eliminate any residual phase error.

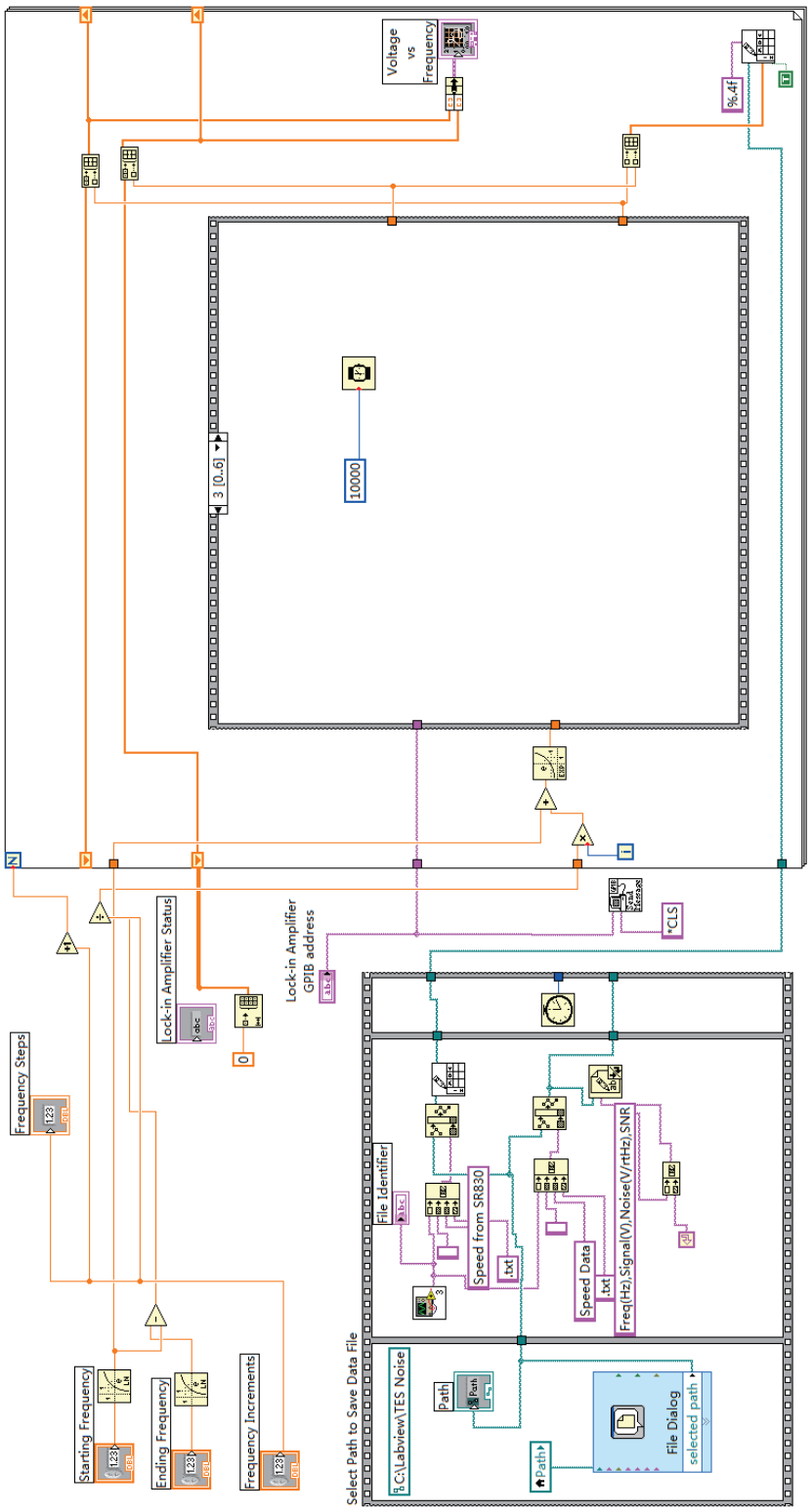

Figure B.22: Labview code for measuring frequency response: step 3. waiting for 10 s.

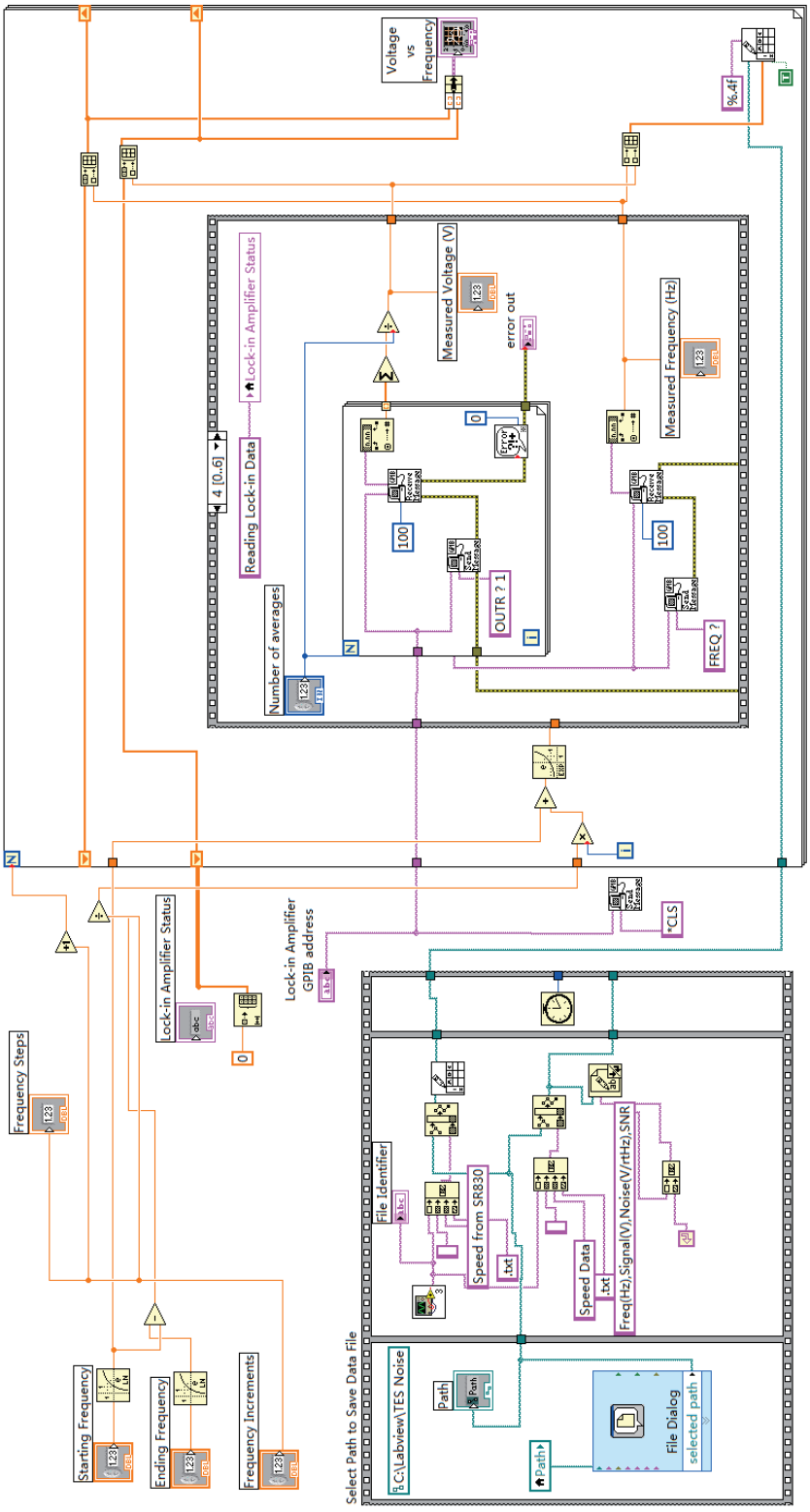

Figure B.23: Labview code for measuring frequency response: step 4. reading both voltage and fequency from the lock-in amplifier.

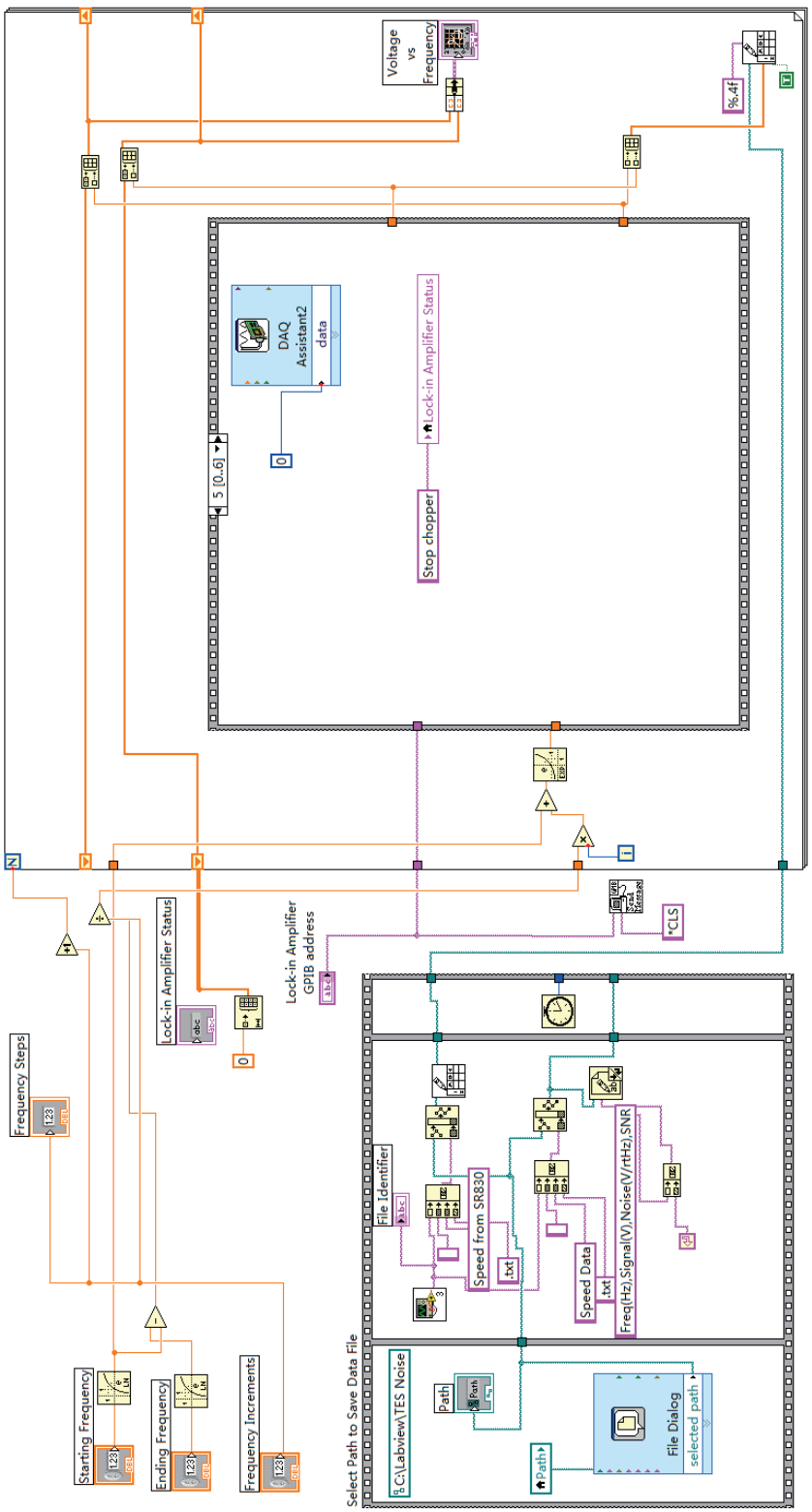

Figure B.24: Labview code for measuring frequency response: step 5. stop the chopper.

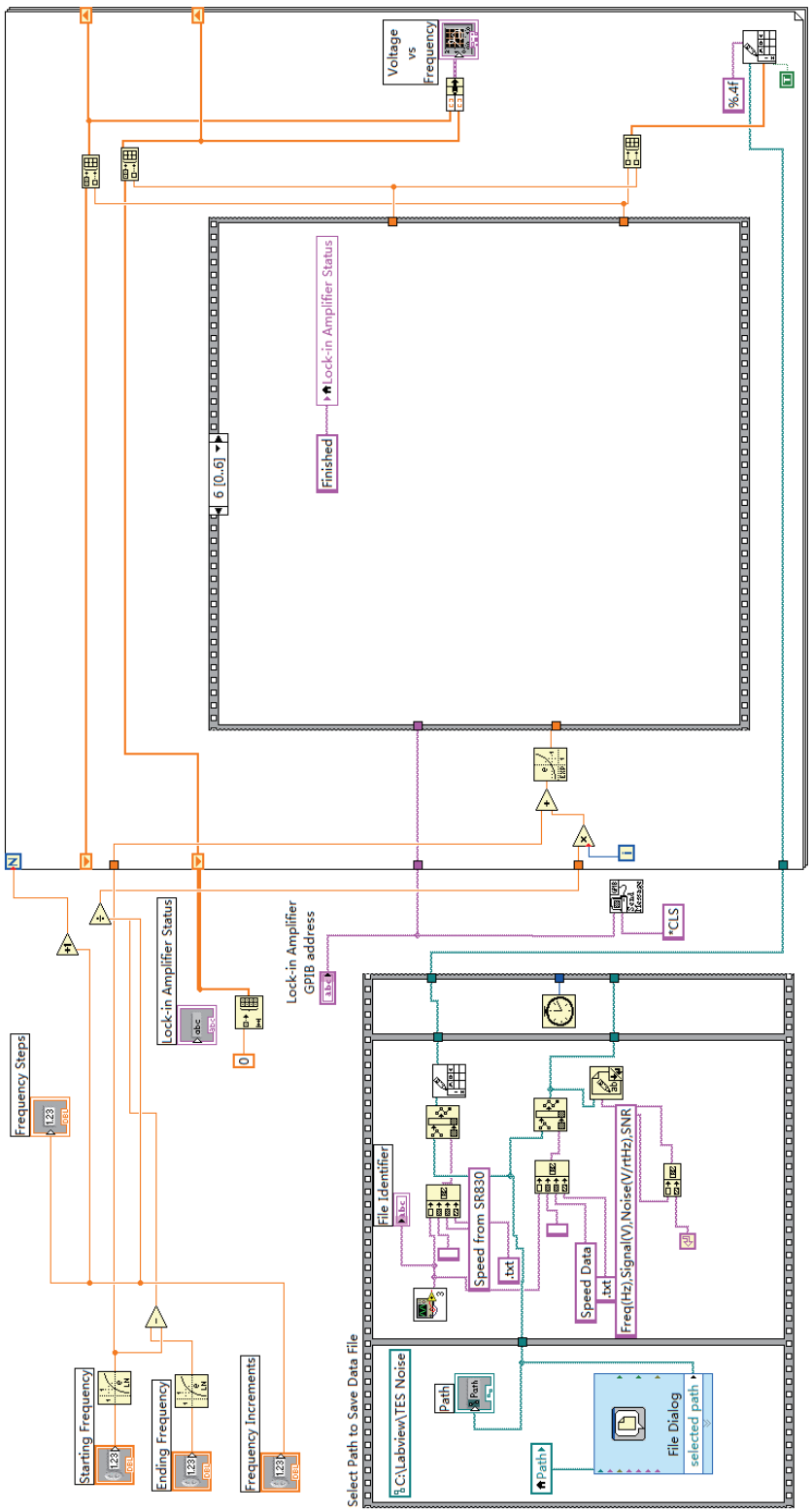

Figure B.25: Labview code for measuring frequency response: step 6. measurements finished.

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